Micro 611: Tunnel FETs
Lecture #4

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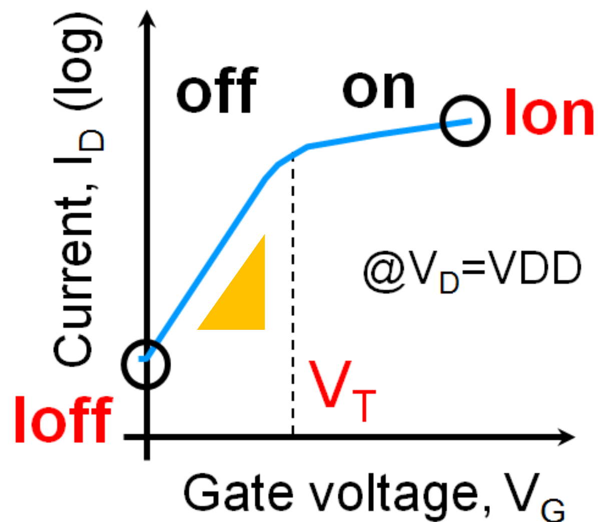
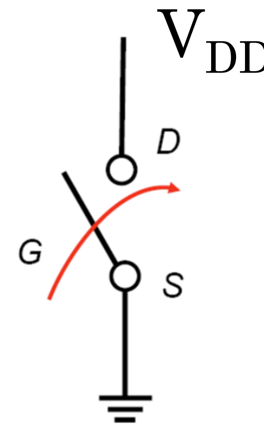
Outline

- Steep slope devices as energy efficient switches
- Tunnel FET principle, optimization and modeling
- Homojunction Tunnel FETs
- Heterojunction Tunnel FETs
- Sub-10mV/dec steep slope: Electron-Hole Bilayer Tunnel FET
- Analog Tunnel FETs
- Conclusions

Steep slope devices as energy efficient switches (1)

- CMOS was historically optimized for performance not for energy efficiency
- Fundamental limits not enough explored
- Swing abruptness by device physics: **off to on**





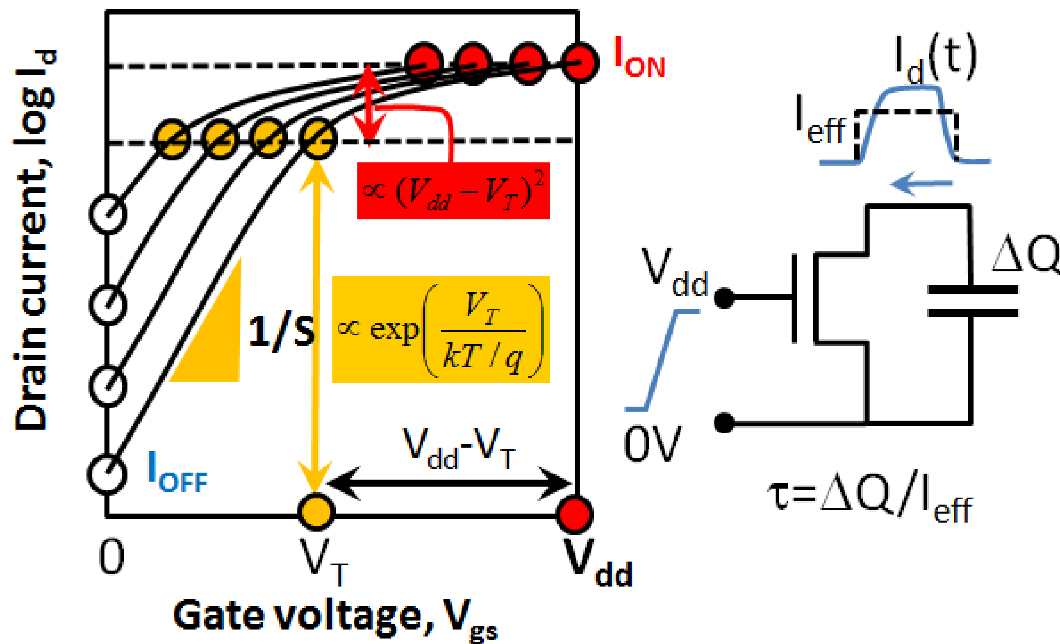
$$S_{avg} = \left(V_T - V_{Goff}\right)/\log(I_T / I_{off}) \approx V_{dd}/\log(I_{on} / I_{off}) \quad \text{[mV/decade]}$$

Important: the average swing over >4 decades of current

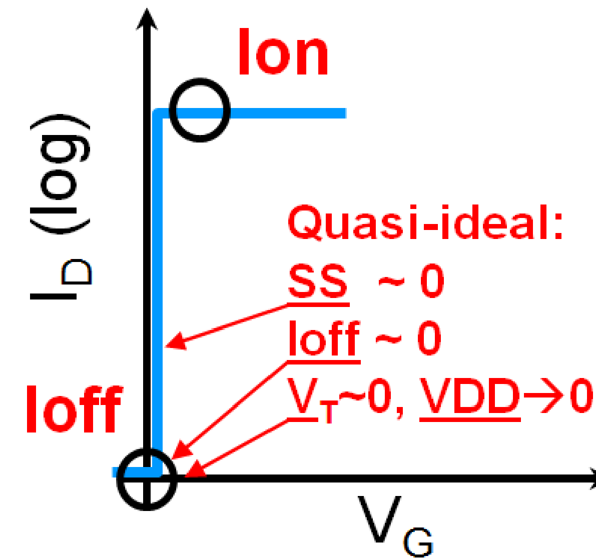
Steep slope devices as energy efficient switches (2)

MOSFET:

- Reducing threshold voltage **by 60mV**
- increases the leakage current **by ~10 times**



Ideal steep slope switch



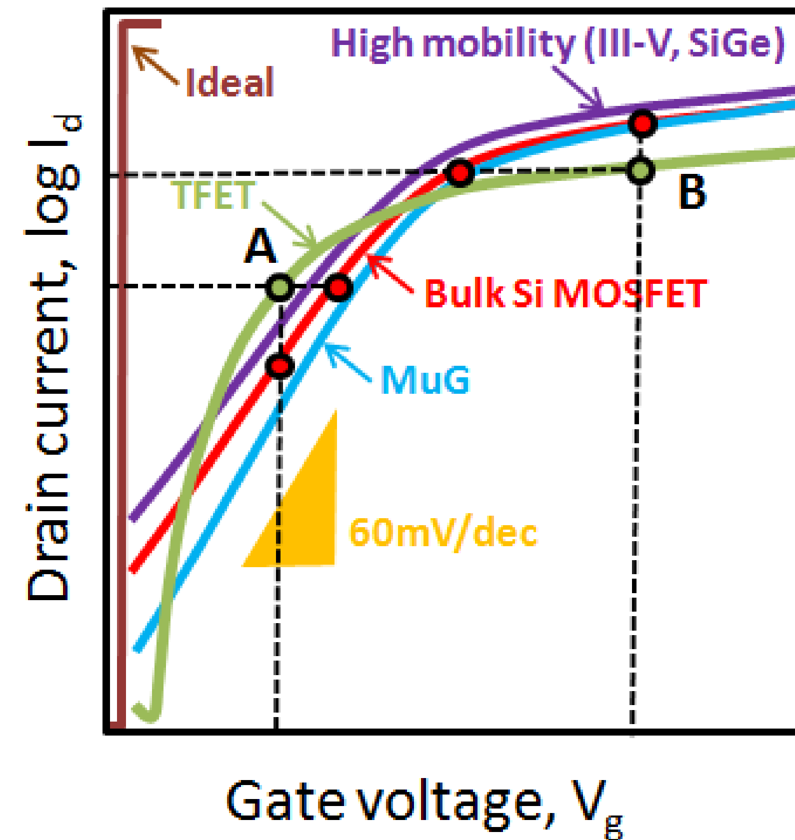
Steep slope definition:
Smaller than 60mV/decade @ 300K

Steep slope devices as energy efficient switches (3)

$$P = \alpha L_D C V_{dd}^2 f + I_{off} V_{dd} \approx K C V_{dd}^{\beta} + I_{off} V_{dd} \quad with\ \beta \simeq 3$$

Key aspects

- Exploit all optimized engineering of MOSFET: nanowires, multigate, high-k
- Exploit **new device physics**
- Should be integrated on CMOS platform and offer design option for LP, ULP: extend the design space of current silicon CMOS.
- Expected advantages:
  - Voltage scaling by **5x** with negligible leakage power could offer a **power reduction > 100x**
  - Energy efficient IC design



Re-engineering the transistor swing @ device level by new physics

Subthrehold swing expression reflects channel injection/transport and gate control.

$$S = \frac{\partial V_g}{\partial(\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_S}}_{m} \underbrace{\frac{\partial \psi_S}{\partial(\log I_D)}}_{n} = (1 + \frac{C_s}{C_{ins}})\frac{kT}{q}\ln 10$$

***m* less than 1**
= active gate devices:

- Negative capacitance
- Electromechanical relay

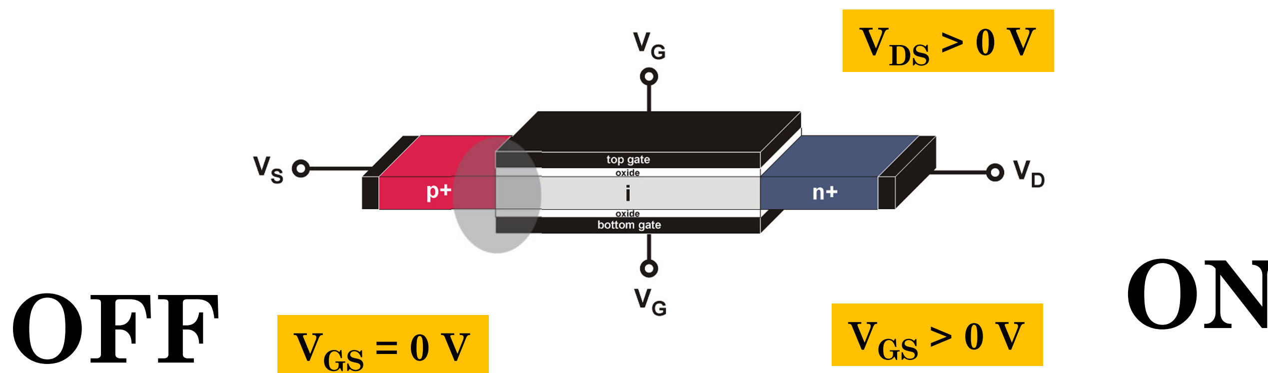
***n* less than (kT/q)ln10**
= new channel injection mechanisms

- **Tunnel FETs**
- Impact Ionization MOS

More radical change:
Metal-Insulator-Transition switch

Tunnel FET principle

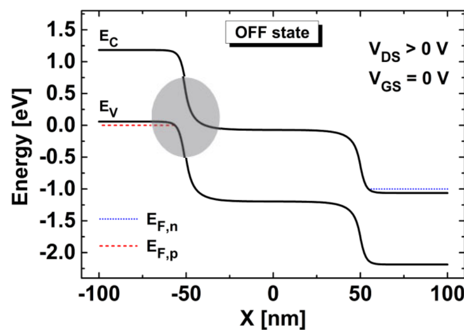
- Exploits **Band-To-Band-Tunneling (BTBT)** in gated reversed biased p-i-n junction (field-effect control of tunneling current)
- Minimum leakage determined by **band gap**



OFF

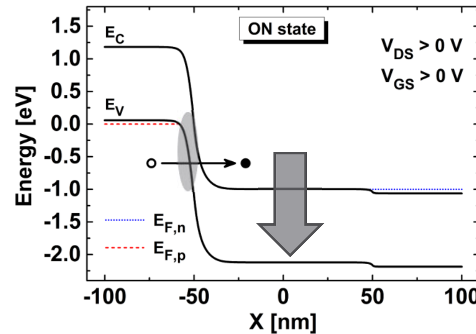
$V_{GS} = 0$ V

Energy barrier **WIDE**
No tunneling



ON

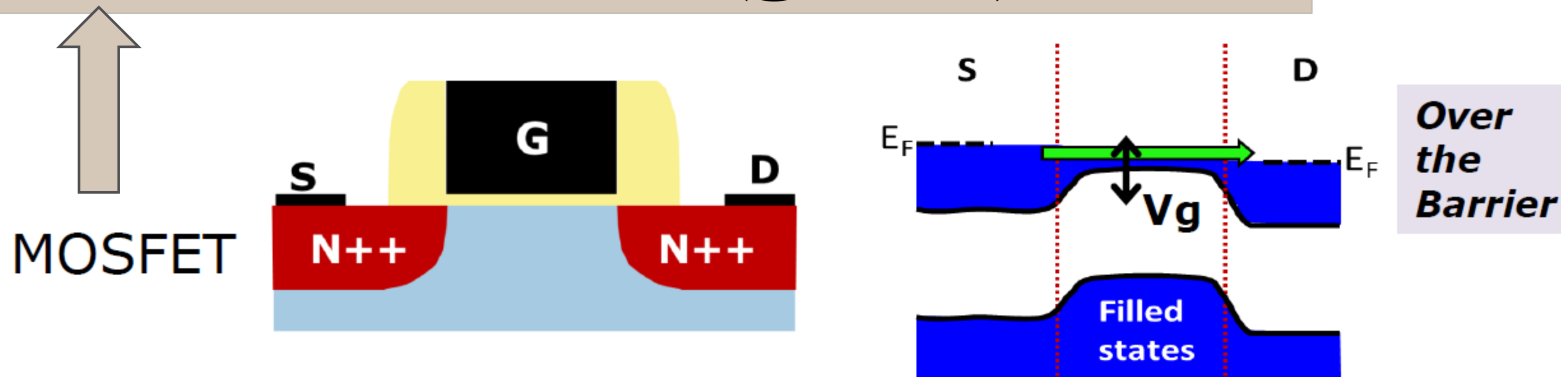
$V_{GS} > 0$ V



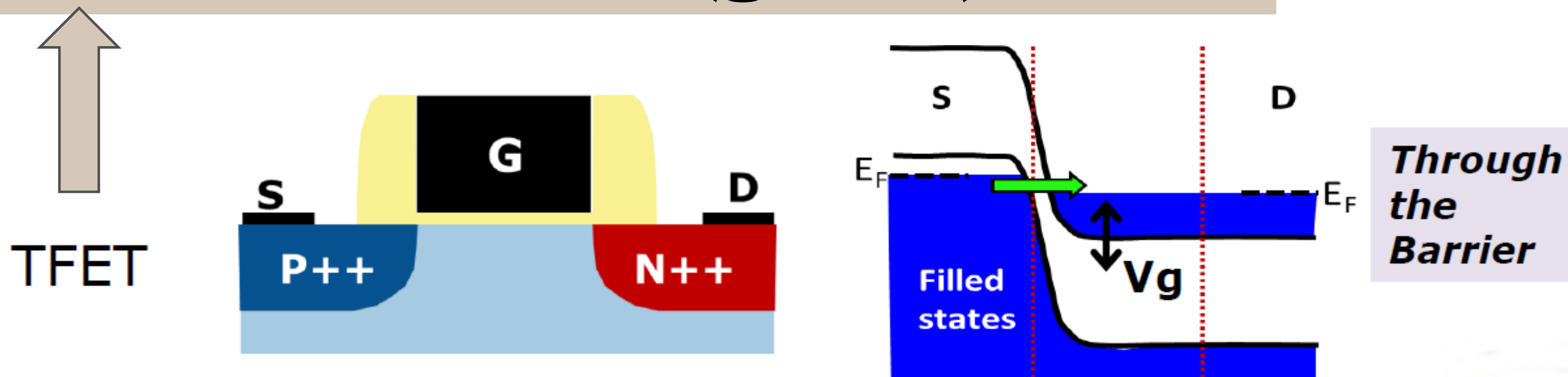
Energy barrier **THIN**
BTB tunneling

Principle: Tunnel FET versus MOSFET

Architecture: N+ / (gated) I / N+



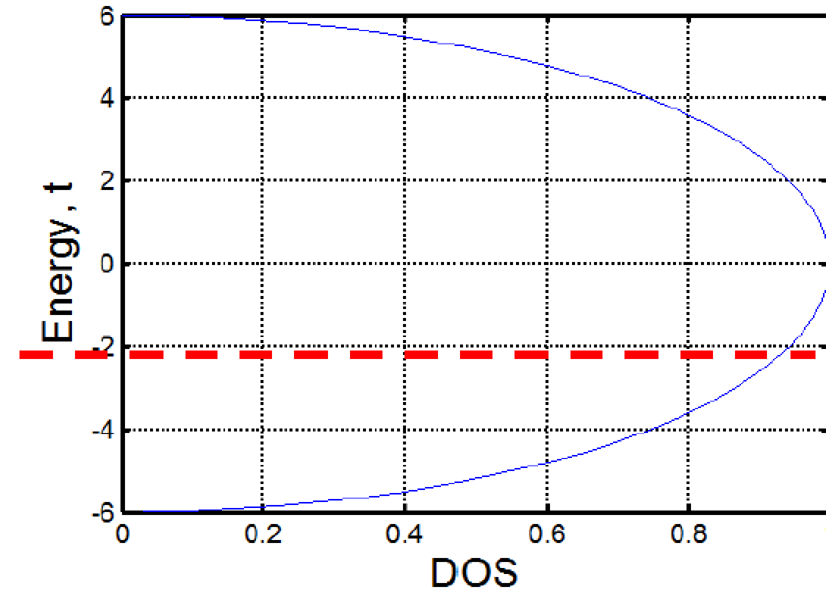
Architecture: P+ / (gated) I / N+



Tunneling and Density of States (DOS)

- Tunnel FETs operate by *quantum-mechanical tunneling* through the S or D junction barriers rather than diffusion over the barrier.

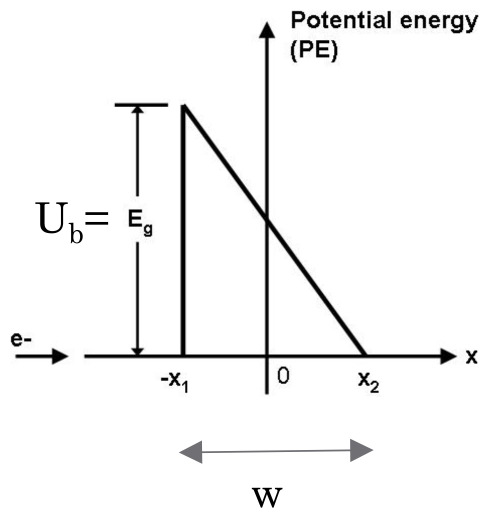
- Two required conditions:
  - ❑ **Thin enough barrier over a large enough area** for effective (high current) tunneling.
  - ❑ **Sufficient density of states on both the transmission and receiving sides** to provide energetic locations for the carriers



$$N \approx \frac{mk_F}{2\pi^2\hbar^2}$$

density of states: larger for a heavy mass

Probability of tunneling



Probability of tunneling through the triangular energy barrier :

$$T \approx \exp\left(-\frac{2w\sqrt{2m_b U_b}}{\hbar} \right)$$

w=width=1nm
mb=mass= 0.2* 9.1*10^{-31}kg
Ub=height=0.8eV
T~0.016

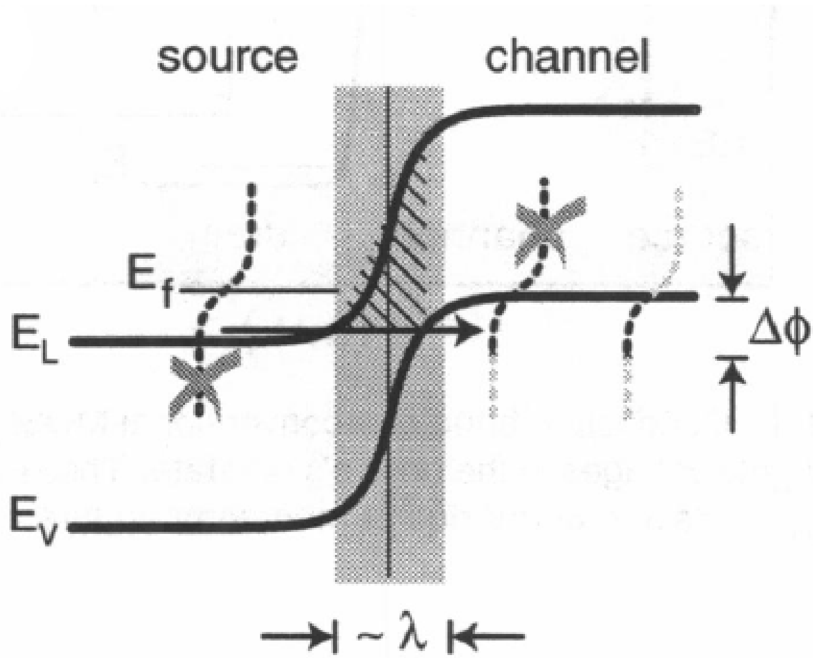
Tunneling current:

$$J \approx \frac{2\pi e^2 V}{\hbar} T U_b^2 N_l N_r a^4$$

N= 4*10^{46} /(J*m^3)
J/V=1.2*10^{14} S/m^2

Source: N. Nikonov, Intel.

BTB tunneling current



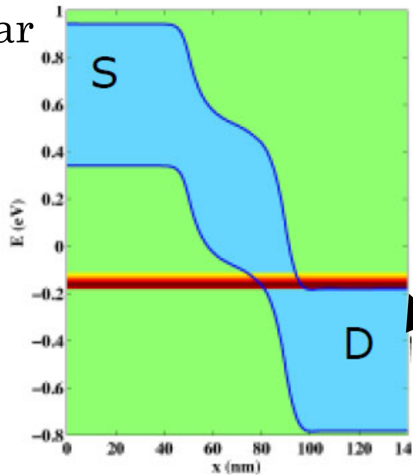
$$I_{BTB} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{1.5}}{3\hbar(\Delta\Phi + E_g)} \right)$$

Parameter	Means of improvement
m*	Small effective tunnel mass, SiGe, III-V, CNT
E_G	Source in SiGe, III-V heterostructures, strain CNT
λ	3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric

Source: H. Riel, IBM.

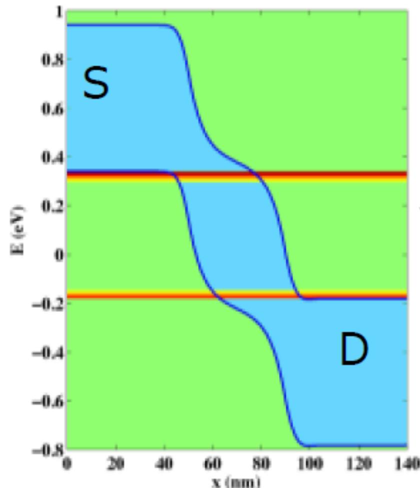
Tunnel FET operation: numerical simulation

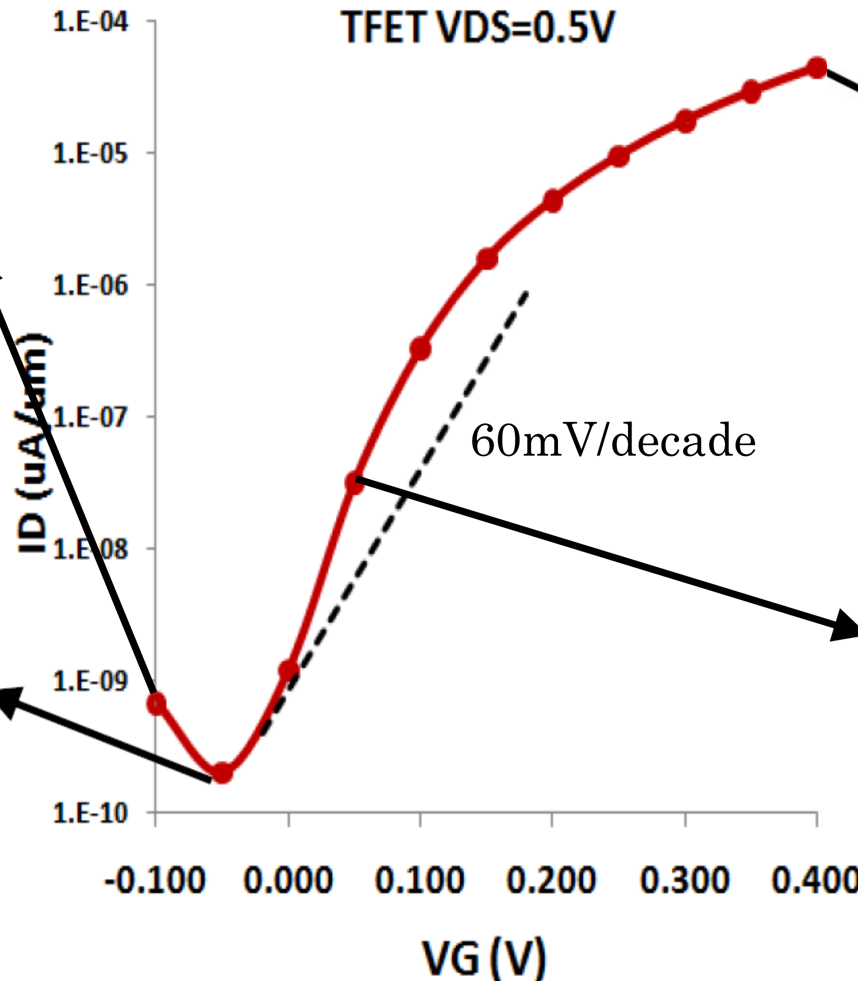
Ambipolar
Opposite
junction

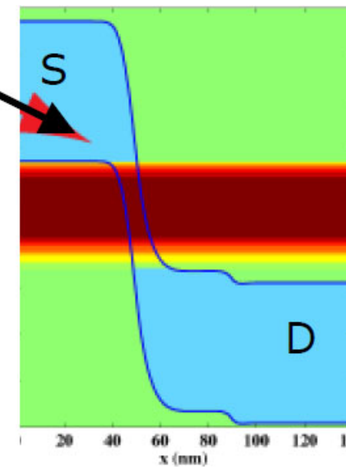


OFF

Wide
barrier,
No
current

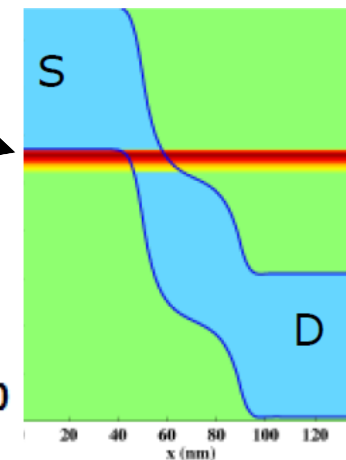






ON

Thin
barrier,
BTB
current
flows

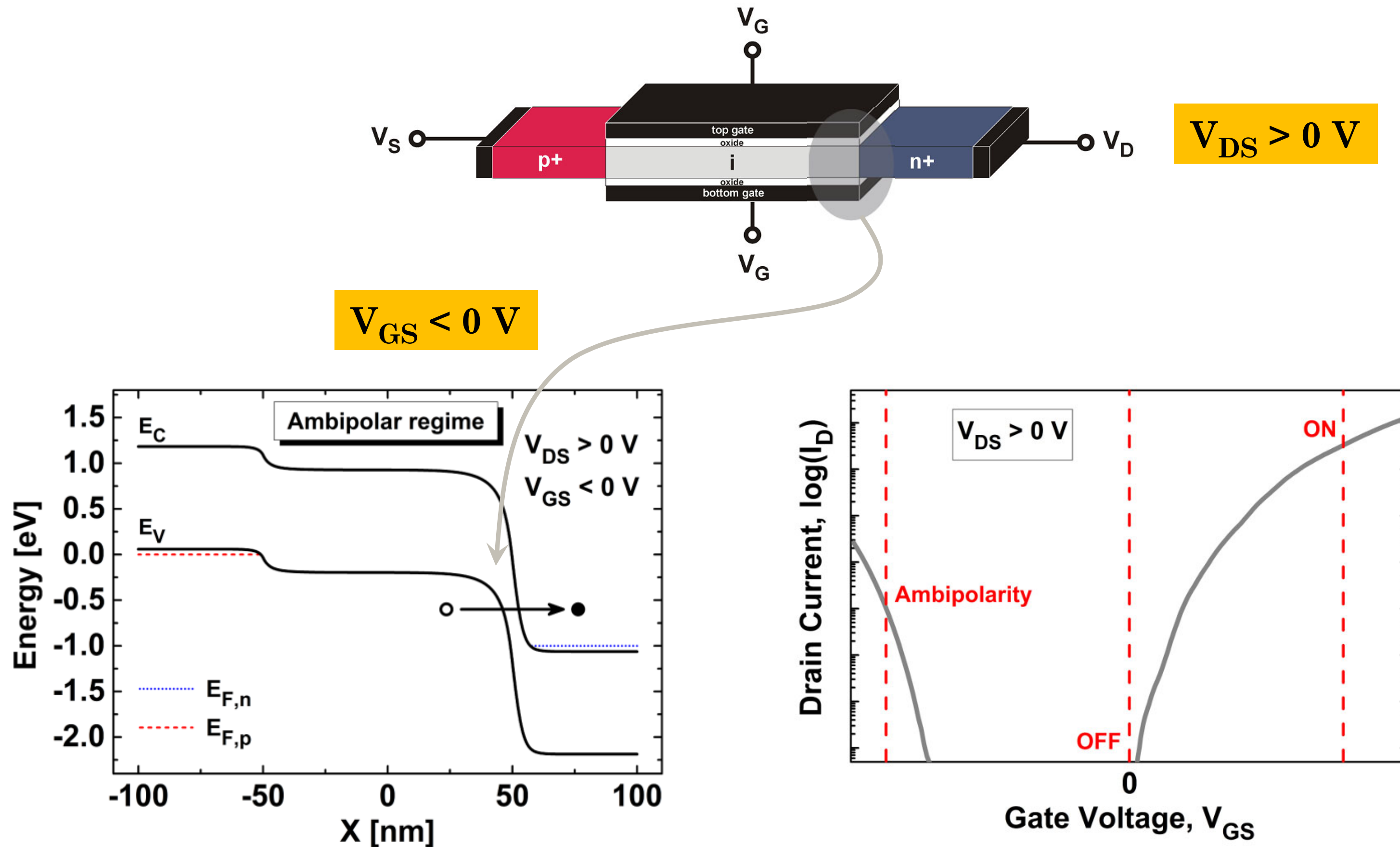


Some
locally
thinned
barrier,
Some BTB
current

Source: M. Luisier and G. Klimeck, IEEE EDL, 30, 602 (2009)

Ambipolar behavior of Tunnel FET

Ambipolar conduction possible in the same device: not good for logic, should be reduced/eliminated



Tunnel FET subthrehold slope modeling

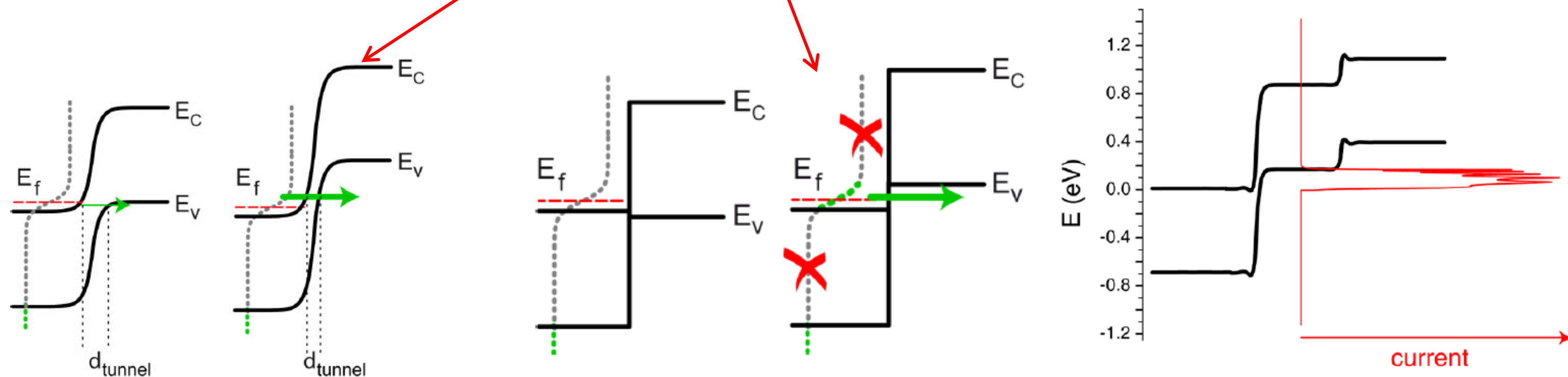
$$I_{\mathrm{d}} = \frac{2e}{h} \int_0^{\Phi_{\mathrm{f}}^0} dE\, T_{\mathrm{WKB}}\left(f_{\mathrm{s}}(E) - f_{\mathrm{d}}(E)\right)$$

$$S = \ln(10)\left(\frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}}\frac{1}{I_{\mathrm{d}}}\right)^{-1}$$

Exponential increase of the current since barrier thinning dominant!

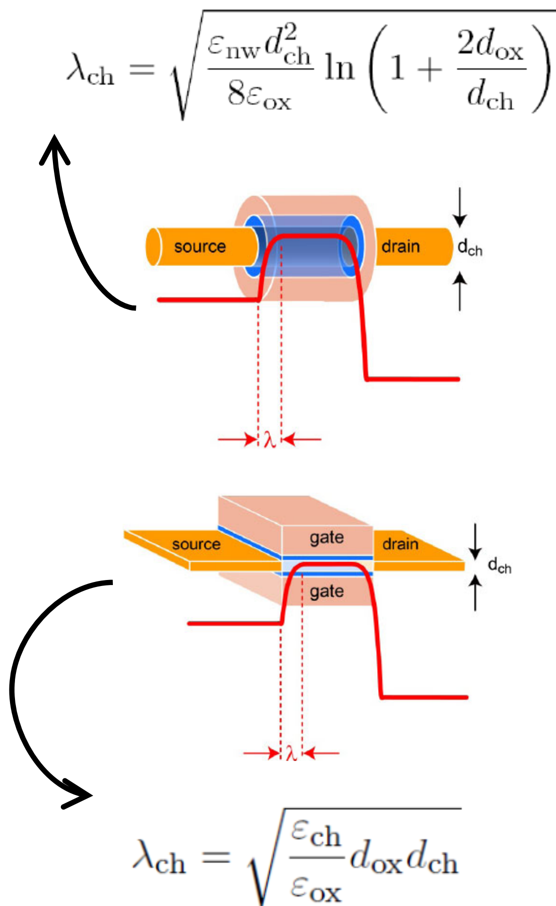
Band-pass filtering behavior

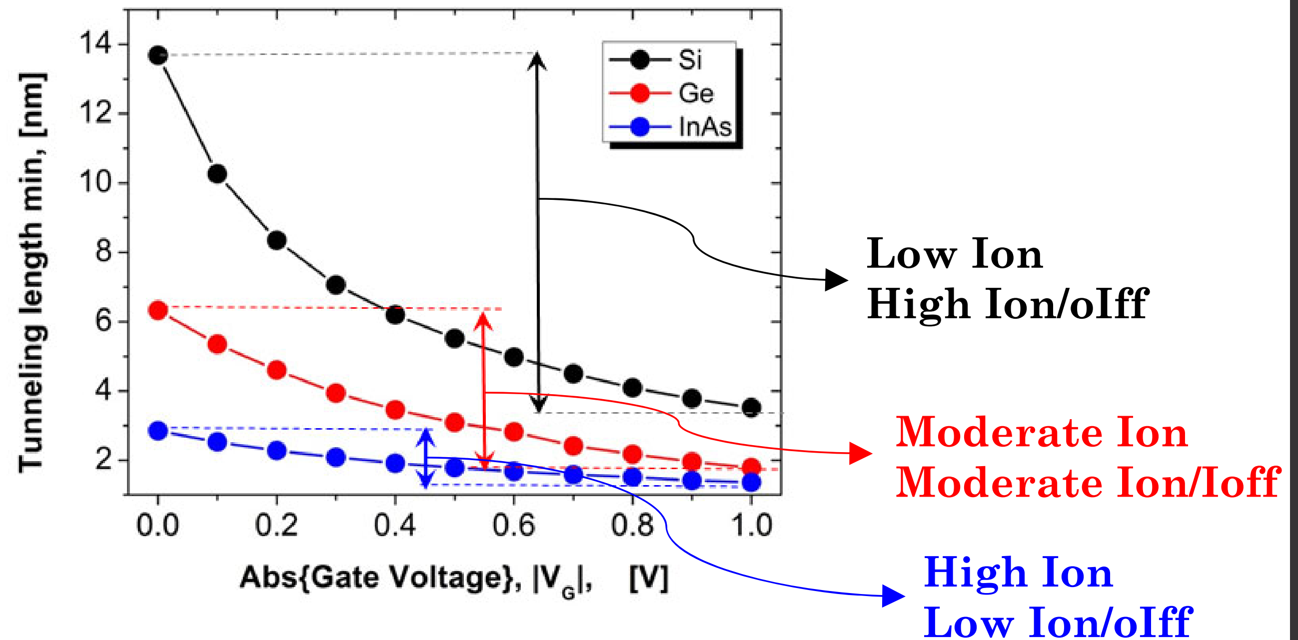
$$S = \frac{\ln(10)}{|e|}\left(\frac{\partial T_{\mathrm{WKB}}/\partial \Phi_{\mathrm{f}}^0}{T_{\mathrm{WKB}}} + \frac{\partial F(\Phi_{\mathrm{f}}^0)/\partial \Phi_{\mathrm{f}}^0}{F(\Phi_{\mathrm{f}}^0)}\right)^{-1}$$



J. Knoch, S. Mantl and J. Appenzeller, Solid-State Electron., 2007.

Tunnel FET, screening length & semiconductor material

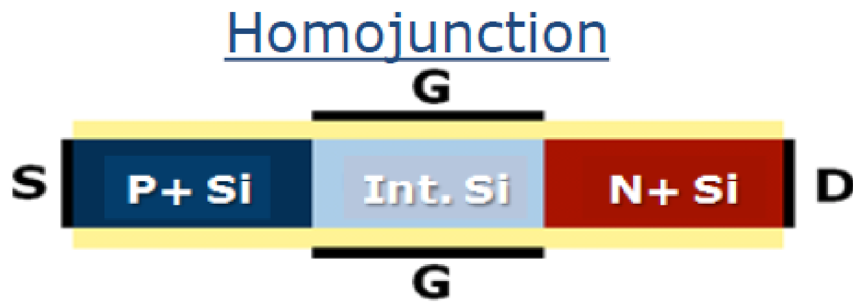


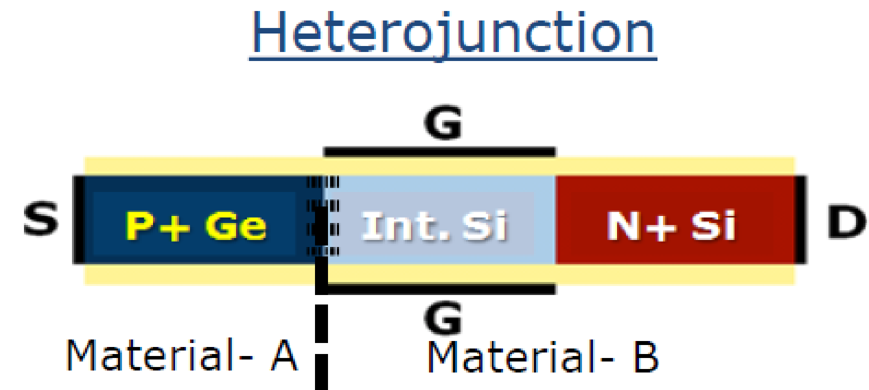


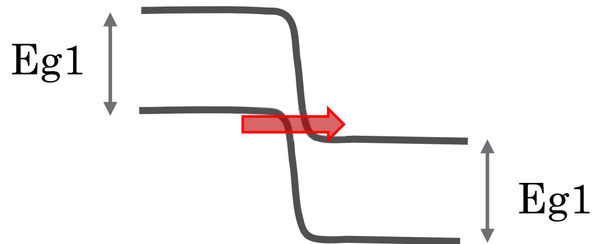
Tunnel FETs need simultaneous optimization of:

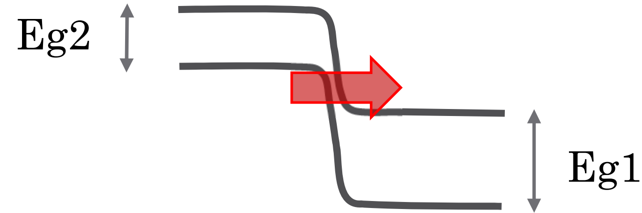
- gate dielectric (thickness, high-k permittivity)
- silicon film thickness (2D material, NW)
- multi-gate: GAA the best!
- fringing fields (high-k/low-k design)
- material choice: low I_{off}, high I_{on}, I_{on}/I_{off}

Homojunction vs. Heterojunction Tunnel FETs



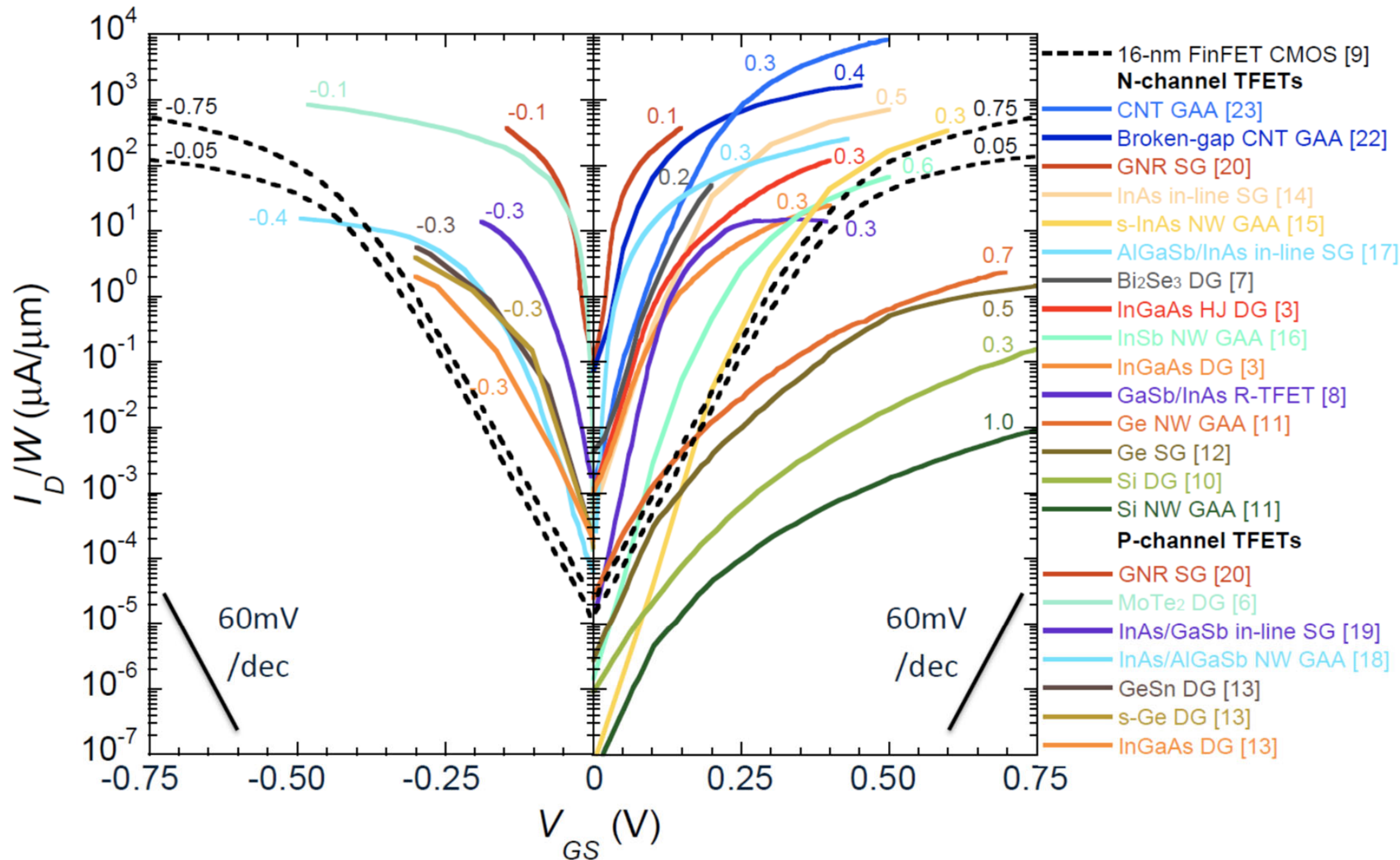






Heterojunction Tunnel FET can achieve much higher tunneling currents.

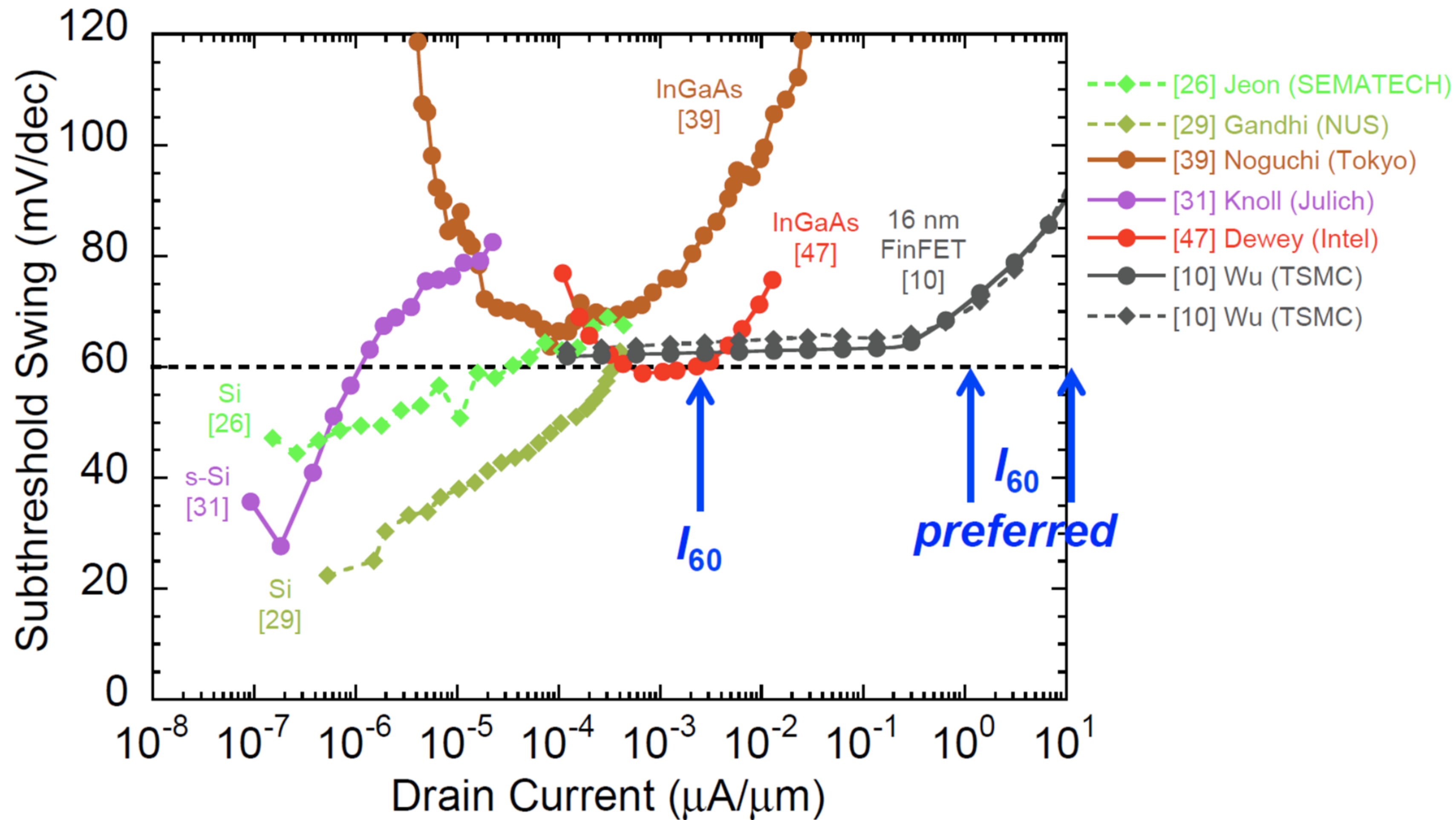
Tunnel FET state-of-the-art - simulations



Simulations generally neglects: band tails due to phonons and heavy-doping, defect-assisted tunneling, interface and border traps

Source: Alan Seabaugh, Uni. Notre Dame.

Four best TFETs showing subthermal swing

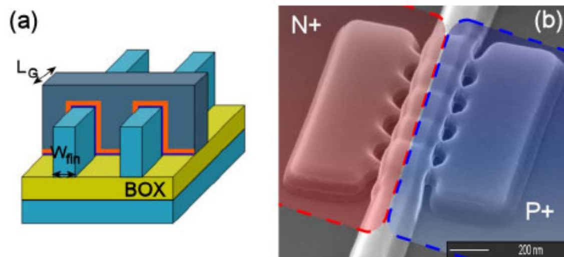


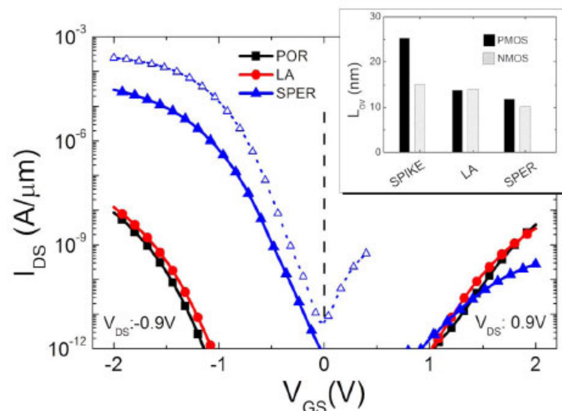
Homojunction Tunnel FETs

Homojunction = junction made of same type of semiconducting materials (all-Si p-n).

FIN Tunnel FETs by IMEC

- **I_{on} =46μA/μm and I_{off}=5pA/μm (V_{DD}=-1.2V)** demonstrated for all-Si devices
- Implant optimization study for junction abruptness (< 3nm/dec)

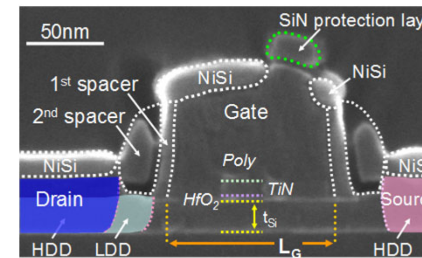


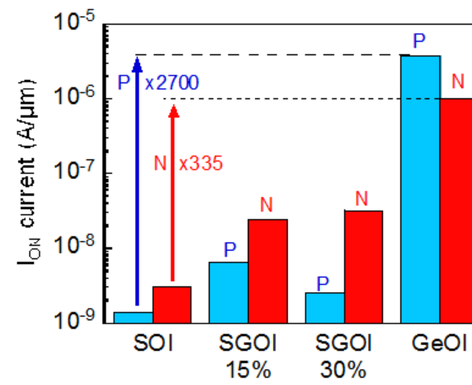


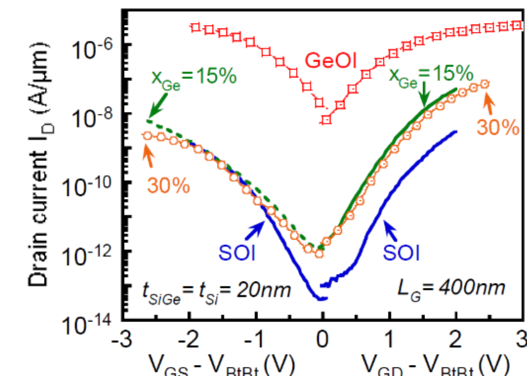
D. Leonelli et al., ESSDERC 2010

DG Tunnel FETs by CEA-LETI

- **Lowest I_{off} in all-Si, S~40mV/dec**
- Significant performance improvement by use of strained SGOI and GeOI
- Ion x 300 (N-type), x 2700 (P-type)
- Trade-off with Ioff: need of heterostructure junctions







C. Leroyer et al., IEDM 2010.

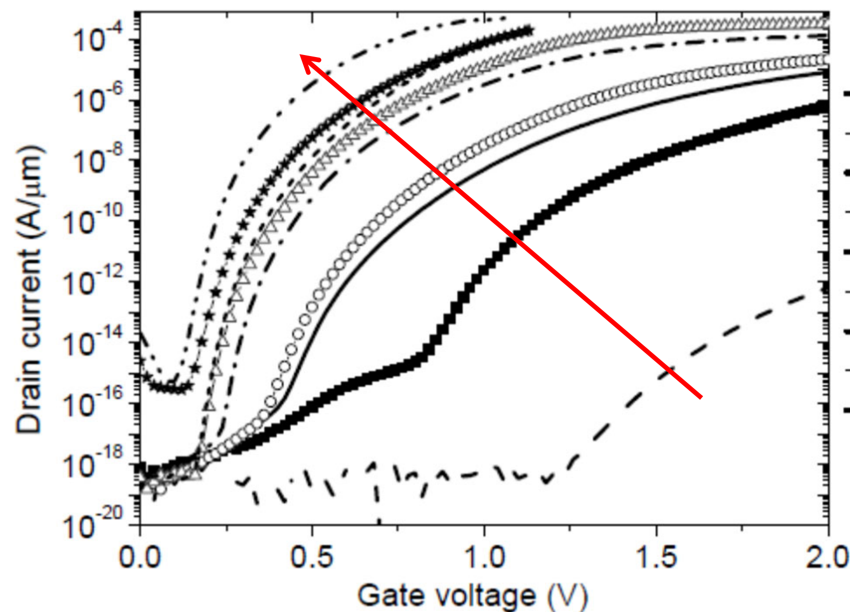
Additive technology boosters for homojunction Tunnel FETs

Technology boosters: similar to the ones of nano-CMOS

Not enough for high performance of **homojunction Tunnel FETs**:

- **S ~ 40-50mV/dec (not steep enough)**
- **Ion ~ 1-10μA/μm (not high enough)**

Need of heterostructures, new materials, with band-gap and gate-alignment optimized design.



A: base device
B: Like A with → **high-k dielectric**
C: Like B with → **narrower junction**
D: Like 'C' with → **thinner body**
E: Like 'D' with → **higher source doping**
F: Like E with → **double gate**
G: Like 'F' with → **oxide /intrinsic reg**.
H: Like 'G' with → **shorter length**.
J: Like 'H' with → **bandgap E_g = 0.8 eV**

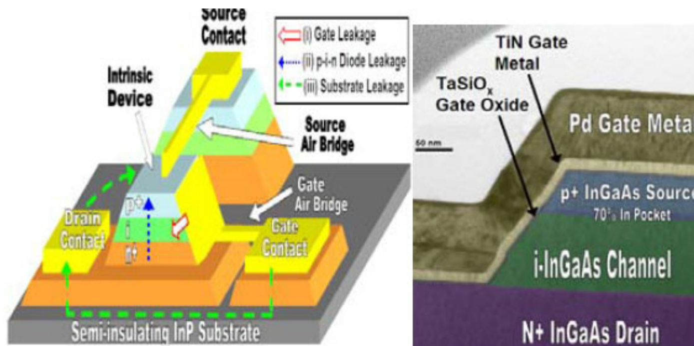
K. Boucart, W. Riess, A.M. Ionescu, ESSDERC 2009.

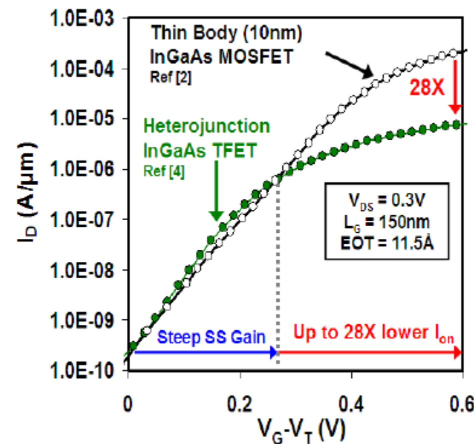
Heterojunction Tunnel FETs

III-V vertical devices with high I_{on} & moderately small subthrehold slope.

Heterojunction Tunnel FET: TaSiOx dielectric, TiN/Pd metal gate and $In_{0.7}Ga_{0.3}As$ pocket

Ion = 1μA/μm; Ioff=200pA/μm;
S < 60mV/dec (Vdd = 0.3V)

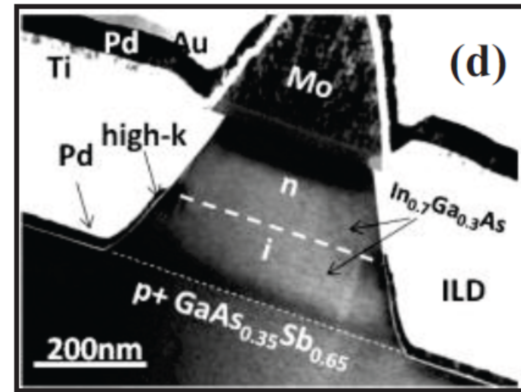


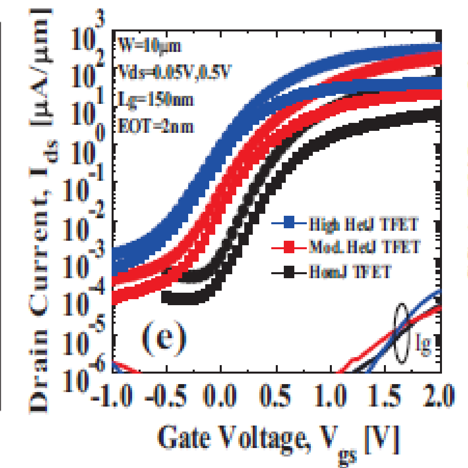


Dewey et al, VLSI 2012 & IEDM 2011.

Staggered tunnel junction ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) heterojunction tunnel FET

Ion=135μA/μm; Ion/Ioff=2.7x10^4;
S=169mV/dec (Vdd=0.5V)





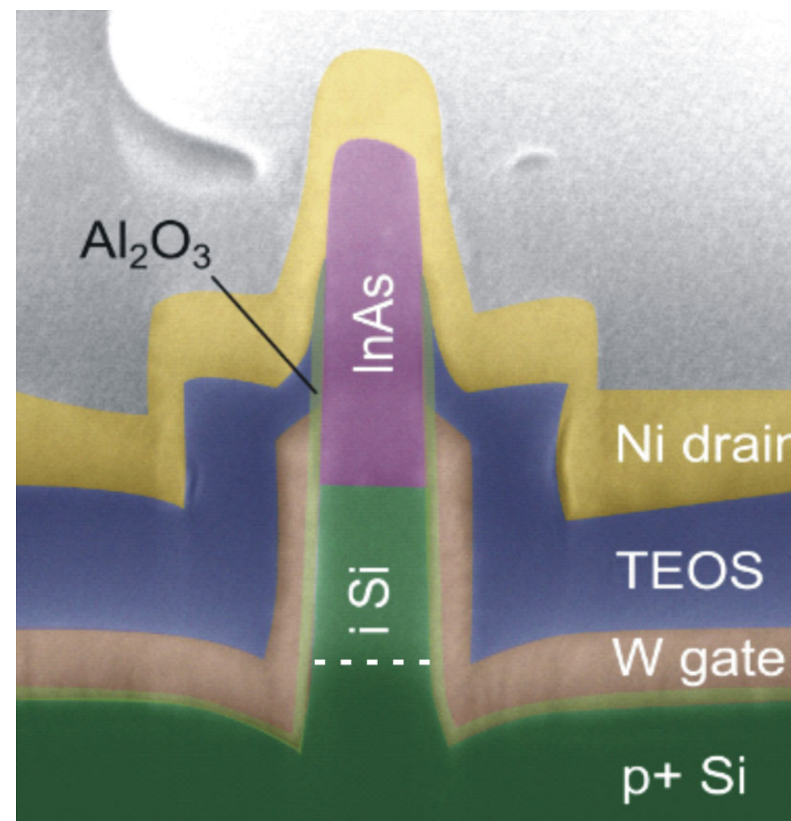
Mohata et al, VLSI 2012.

Scalable high performance heterostructure Tunnel FET

- n-type InAs Source on Si Tunnel FET

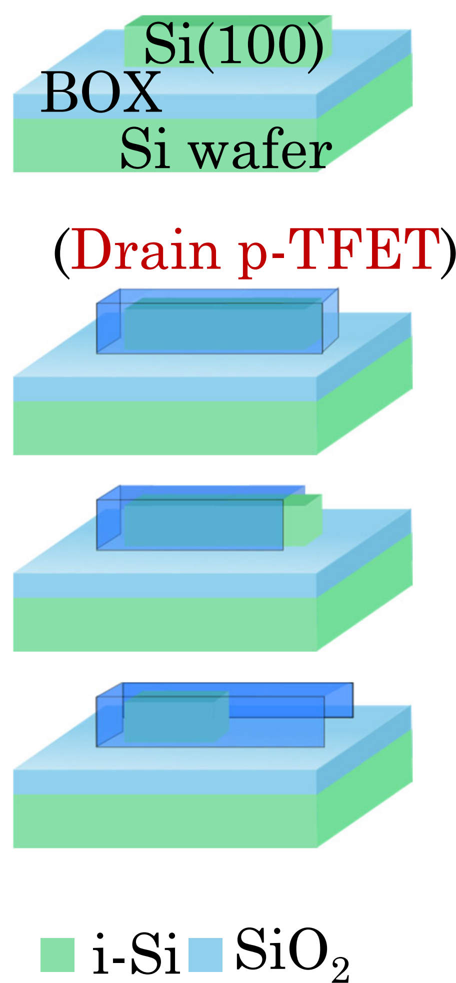
Advantages:
- III-V source: small band-gap, high currents
- Intrinsic Si channel: best dielectric interface (less D_{it})
- GAA architecture: best electrostatic control

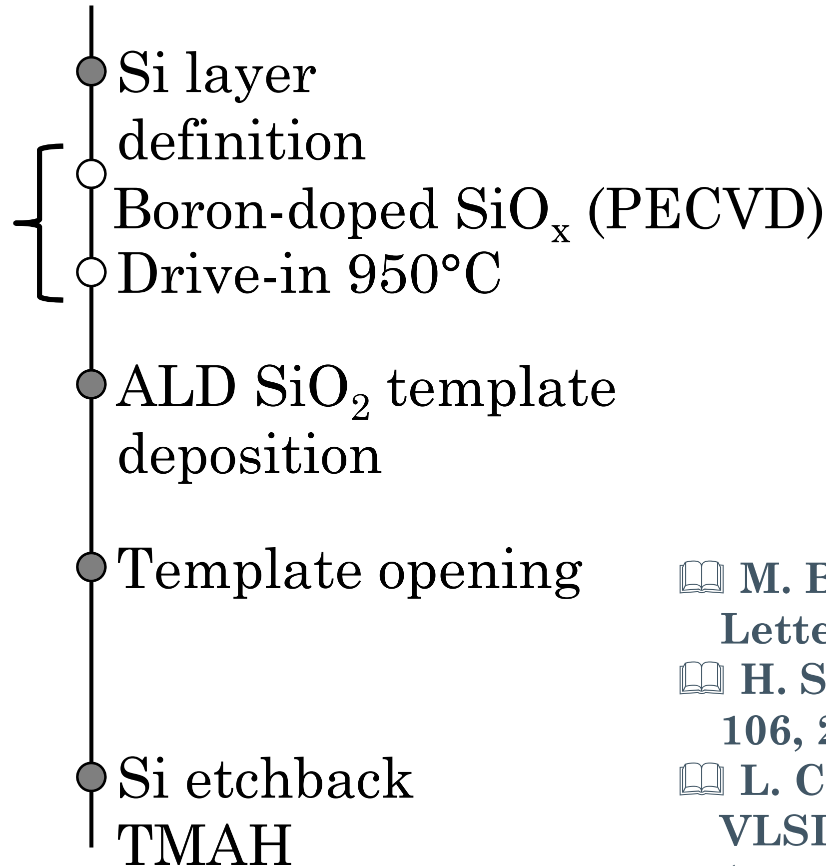
Challenges:
- Integration of InAs on Si with defect-free interface (lattice mismatch InAs/Si 11%)
- Appropriate doping levels in source, channel and drain
- Processing of vertical devices with scaled dimensions



Source: e[2]SWITCH, IBM.

IBM's Horizontal template-assisted selective epitaxy nanowire process for Tunnel FETs

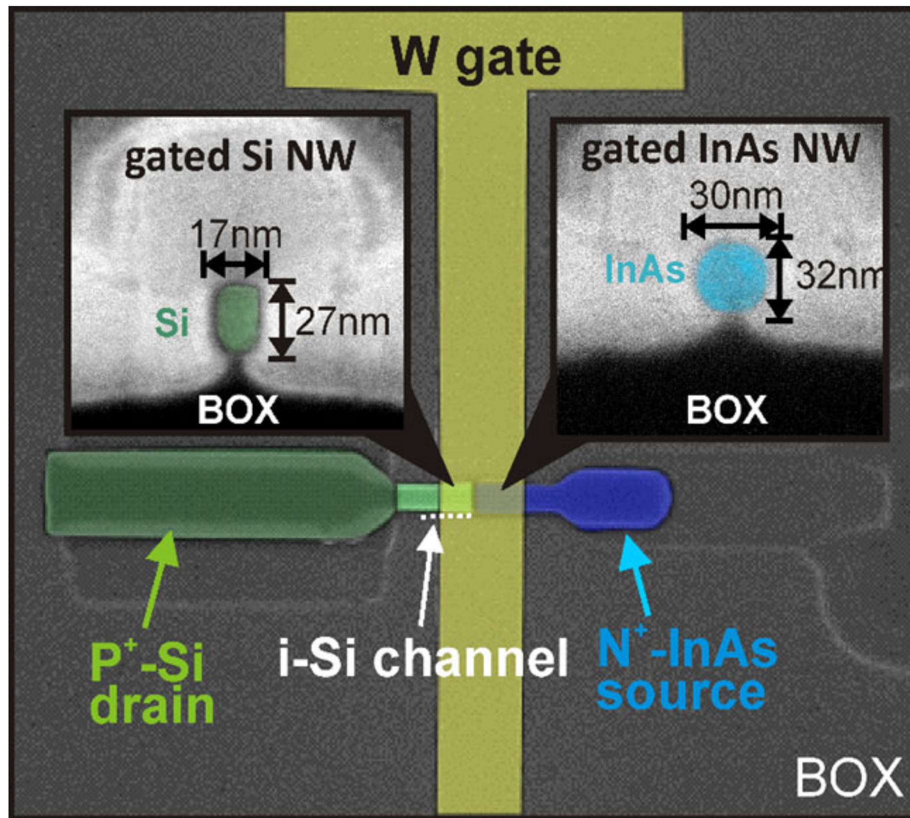




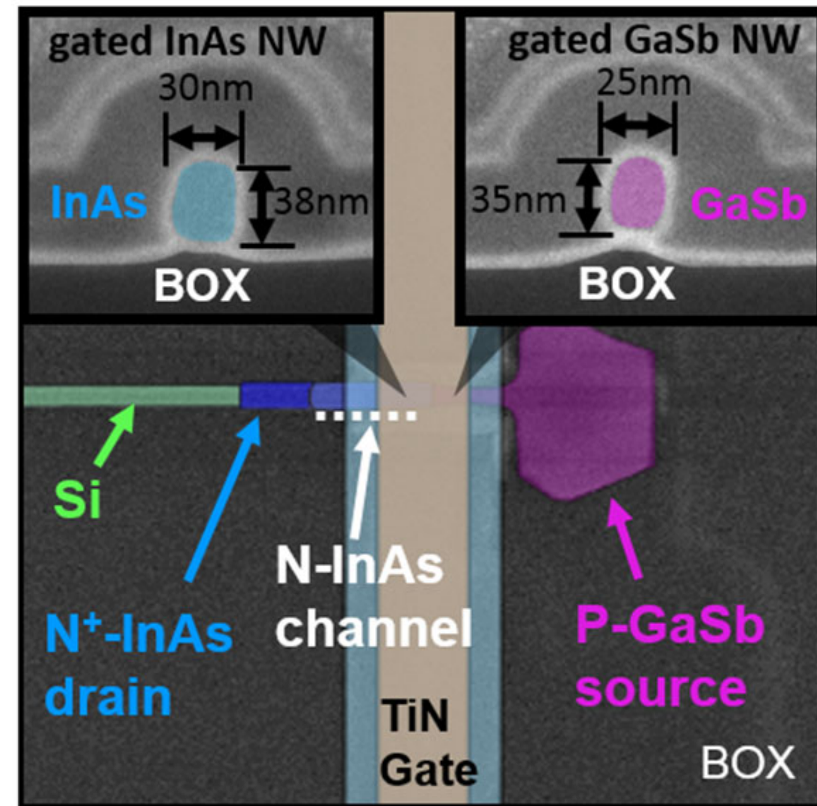
- M. Borg et al, Nano Letters 14, 1914, (2014)
- H. Schmid et al, APL 106, 233101 (2015)
- L. Czornomaz et al, VLSI Symp. T172-T173 (2015)

IBM’s Complementary lateral Tunnel FETs

p-TFETs

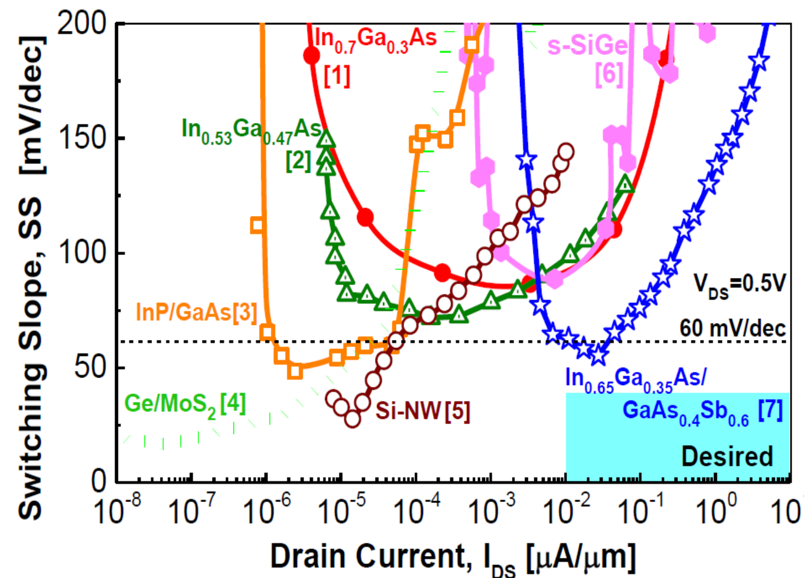


n-TFETs



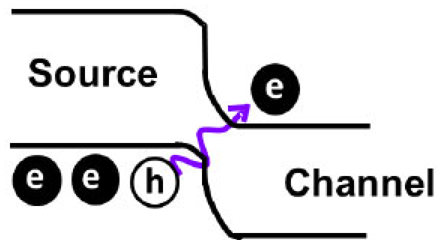
Tunnel FETs: summary of performance

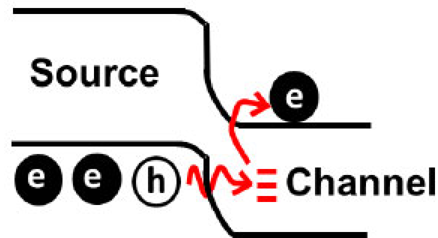
- Many optimizations still needed:
  - III-V provide versatile solutions for high Ion but suffer from unacceptably high Ioff; particularly promising is the staggered/broken type-II GaAsSb/InGaAs heterojunction.
  - Si Tunnel FETs fill the low Ioff region but all-Si homojunction Tunnel FET is not likely to reach the required Ion performance

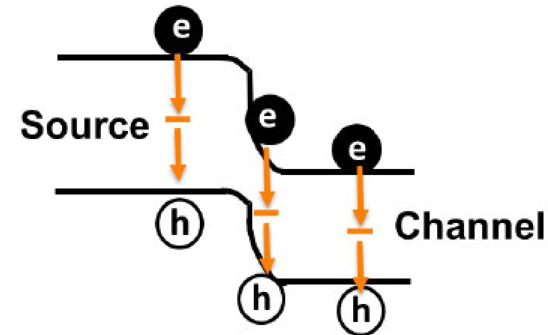


[1] H. Zhao et al, IEEE EDL, Dec. 2010
[2] M. Noguchi et al., IEDM 2013
[3] B. Ganjipour et al., ACS Nano, Apr. 2012
[4] D. Sarkar. et al., Nature Vol. 526, Oct. 2015
[5] L. Knoll et al., IEEE EDL, June 2013
[6] A. Villalon et al., VLSI 2012
[7] R. Pandey et al., VLSI 2015

Big technological challenge for Tunnel FETs: *Trap assisted tunneling*







Band-To-Band-Tunneling (BTBT)

Ideal and Desirable

Trap-Assisted-Tunneling (TAT)

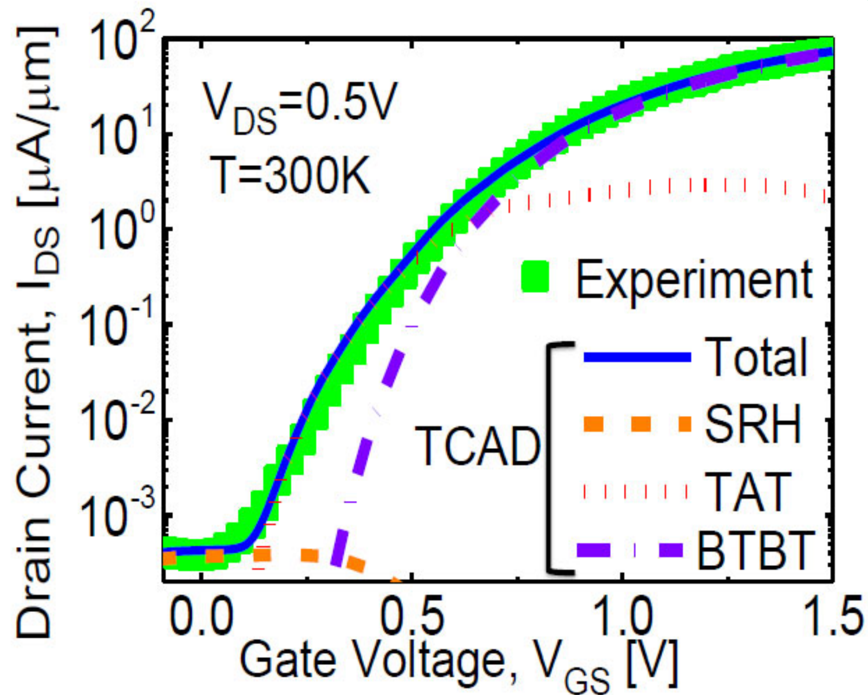
Shockley-Read-Hall recombination (SRH)

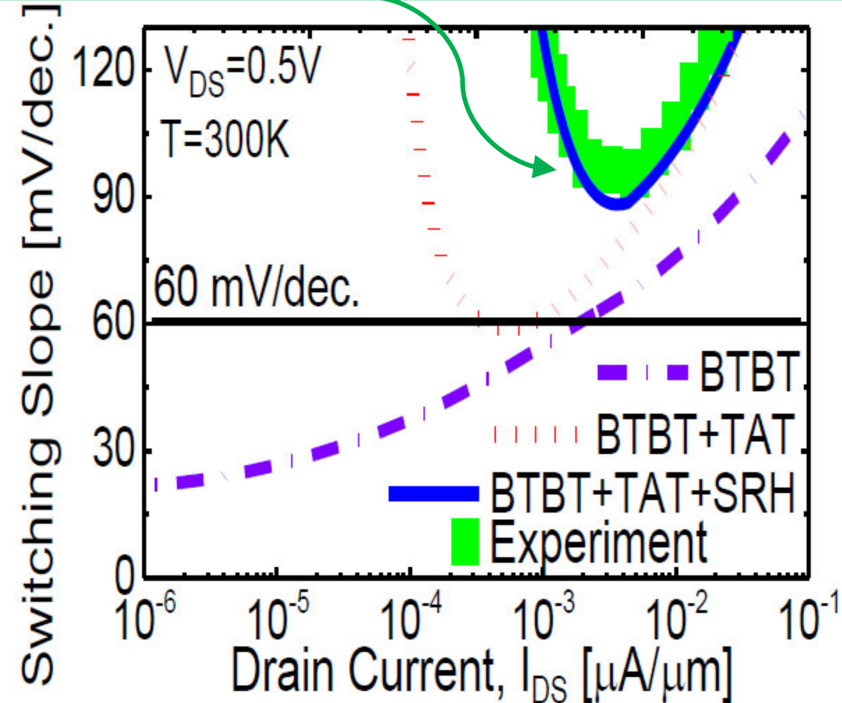
Parasitic and Un-desirable

3 Dominant transport mechanisms in HTFET

Effect of Trap Assisted Tunneling (TAT) on Tunnel FET characteristics

Min of slope dictated by TAT not by BTBT





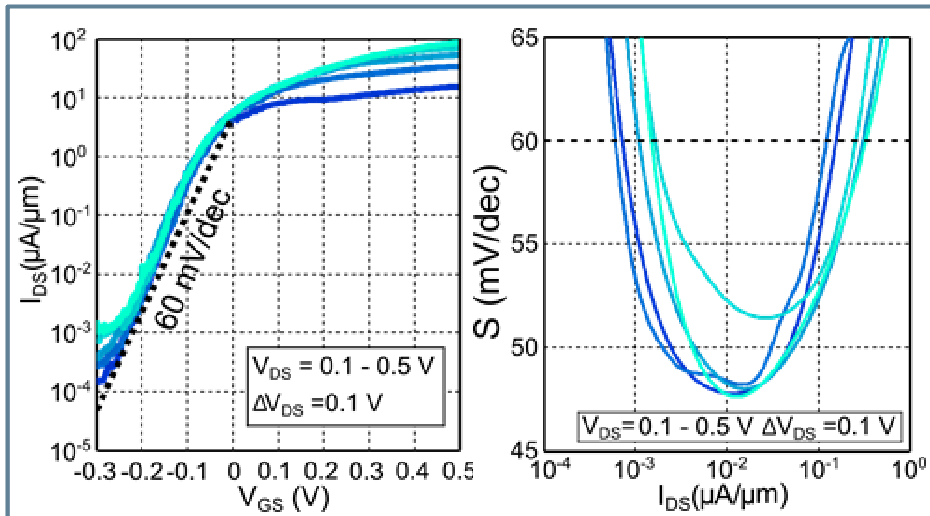
Reduced Dit (TAT), reduced body thickness (SRH) are necessary for demonstrating steep slope TFETs

… and the best experimental Tunnel FET is…

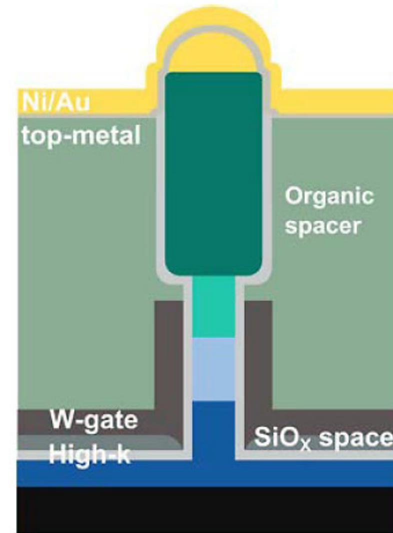
- E²SWITCH Consortium: Uni Lund @ IEDM 2016

  Vertical Heterostructure InAs/GaAsSb/GaSb Tunnel FET

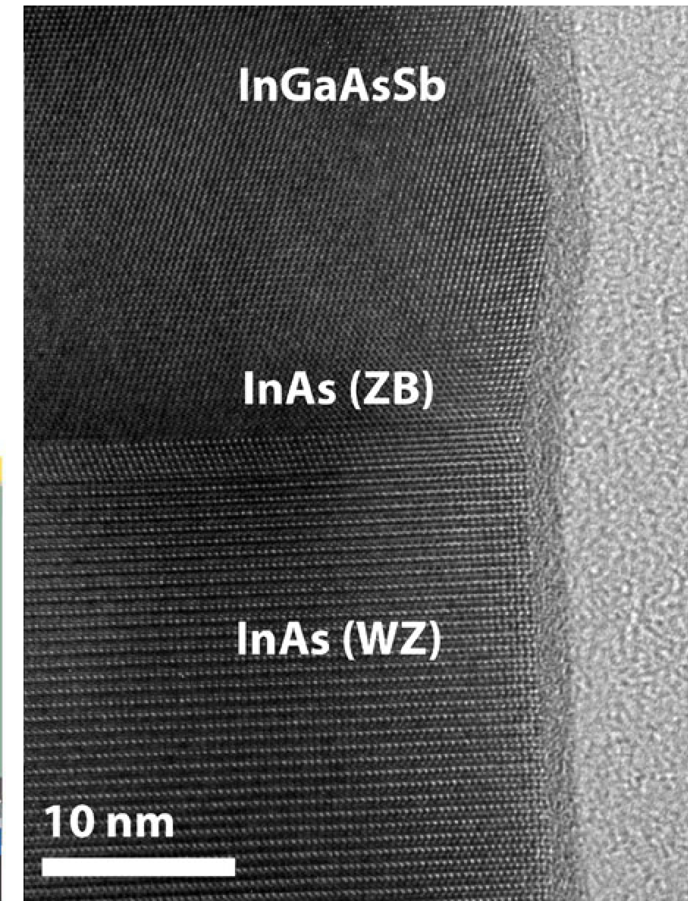
  - **Ioff= 1nA/um, Ion=10.6 uA/um @ Vdd=0.3V**
  - Point SS @ 50mV = 44mV/dec / @ 300mV = 48mV/dec
  - Id @ lowest point SS @ 100mV =6.7 nA/um/ @ 300mV =10 nA/um



E. Memisevic et al., IEDM 2017.



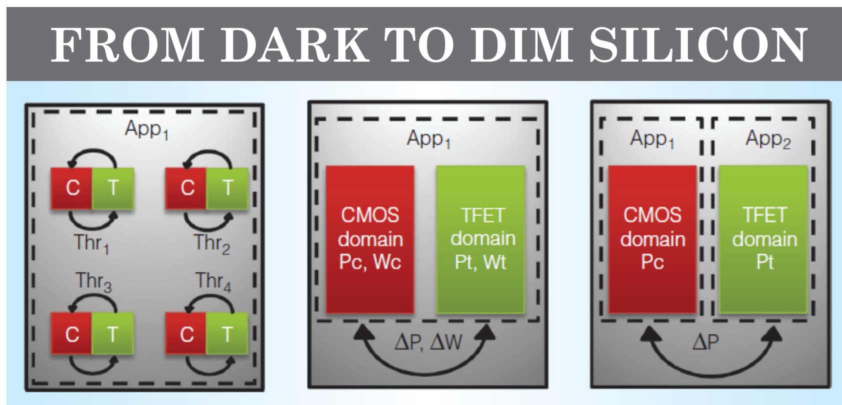
Sharp, low defect heterojunction



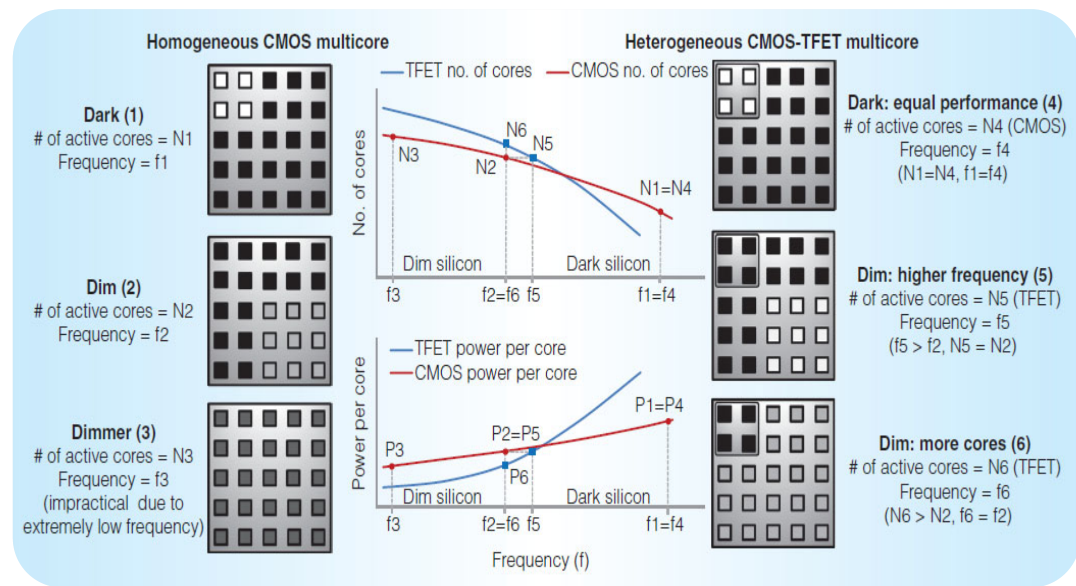
Axel Persson, Lund

Tunnel FET applications in foreseeable future

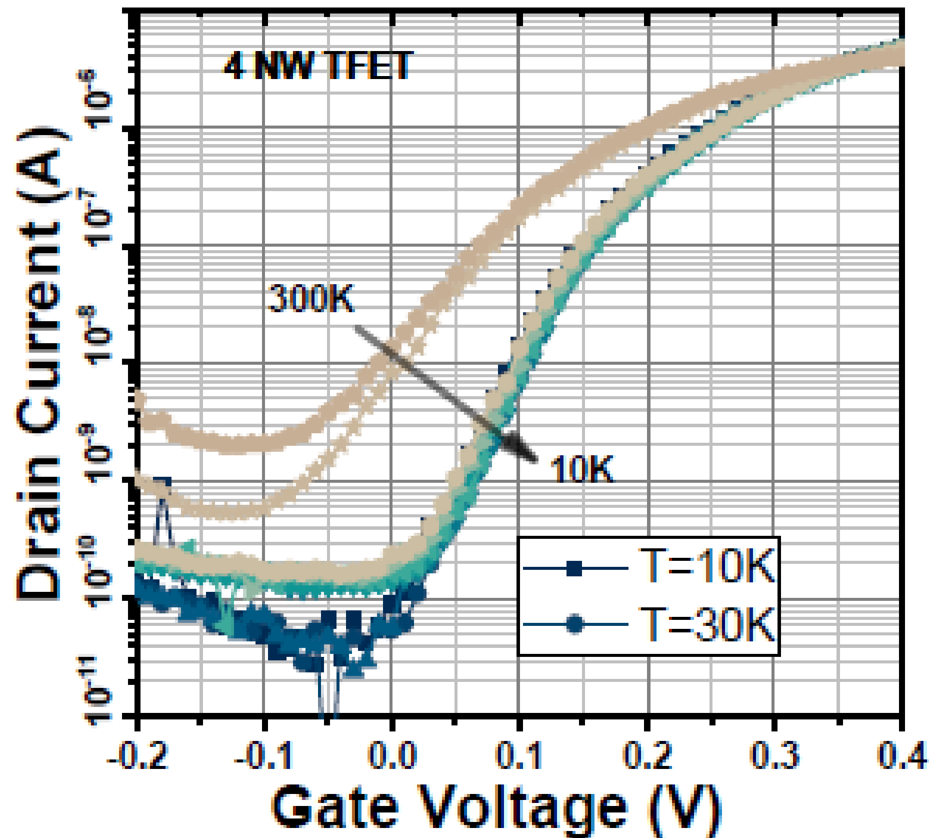
- **Heterogenous CMOS-Tunnel FET multi-core processor design for** *better energy efficiency (up to 50% energy benefits)*
- **IoT sensors nodes based on Tunnel FETs:**
  - Analog/RF Tunnel FETs for energy efficient IoT nodes operating @ 100mV
  - Ultra sensitive new tunnel FET sensors for IoT nodes (<10-100microW/node)
- **Neuromorphic design with Tunnel FETs**



V. Saripalli et al., DAC 2011.
K. Swaminathan, IEEE Computer,

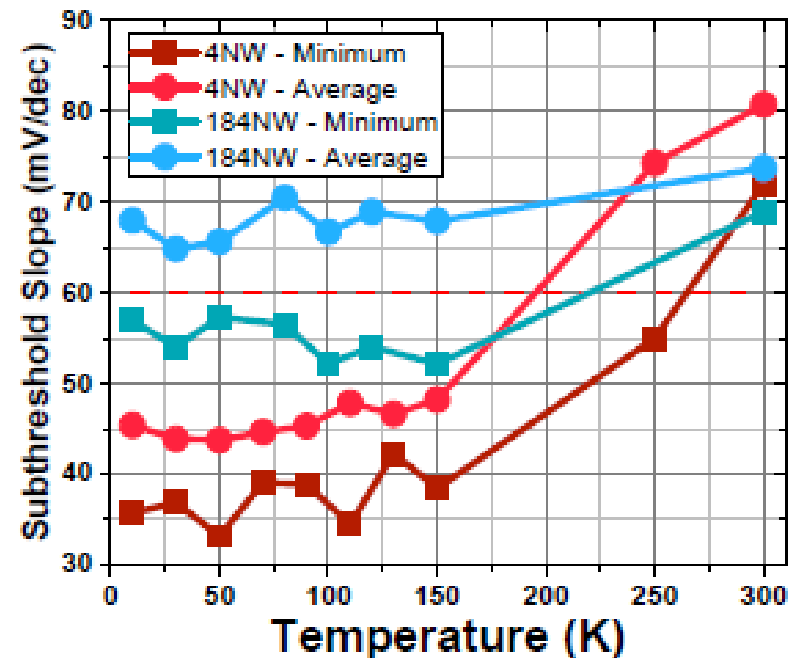


Effect of Trap Assisted Tunneling (TAT) is cancelled at low temperature (<100K)



T. Rosca et al., to appear @ IEDM 2018.

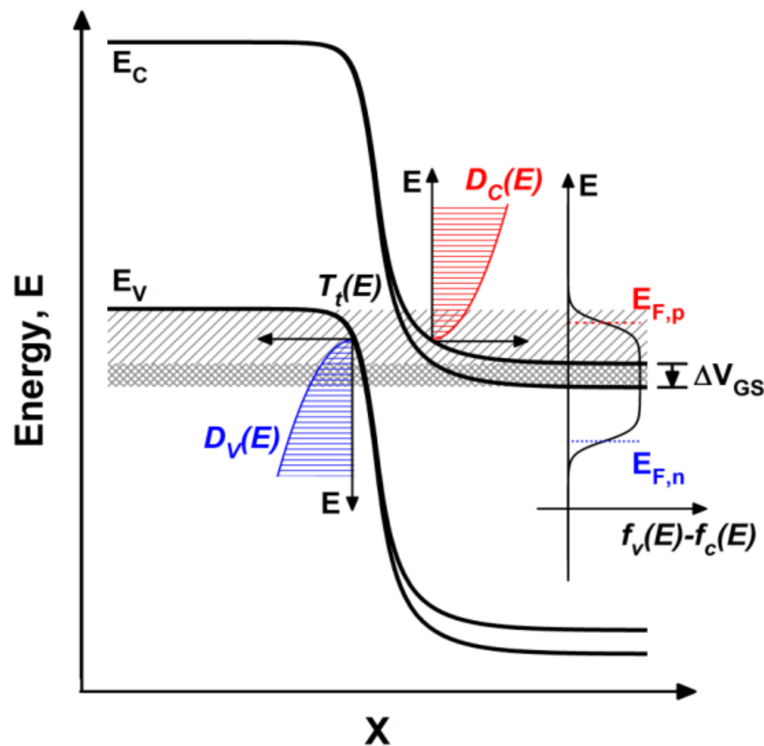
- When dictated ONLY by BTBT, the subthreshold slope dependence on temperature is quasi-negligible.
- TAT effect and dependence on temperature are removed below 100K.



What about a true deep-subthermal swing: like S < 10mV/decade at room temperature over > 4 decades of drain current ?

The Density of States (DOS) switch

$$I_t \propto \int_{E_C^{ch}}^{E_V^{s}} \underbrace{T_t(E)}_{\text{I}} \underbrace{[f_V^{s}(E) - f_C^{ch}(E)]}_{\text{II}} \underbrace{D_V^{s}(E)\, D_C^{ch}(E)}_{\text{III}} \, dE$$



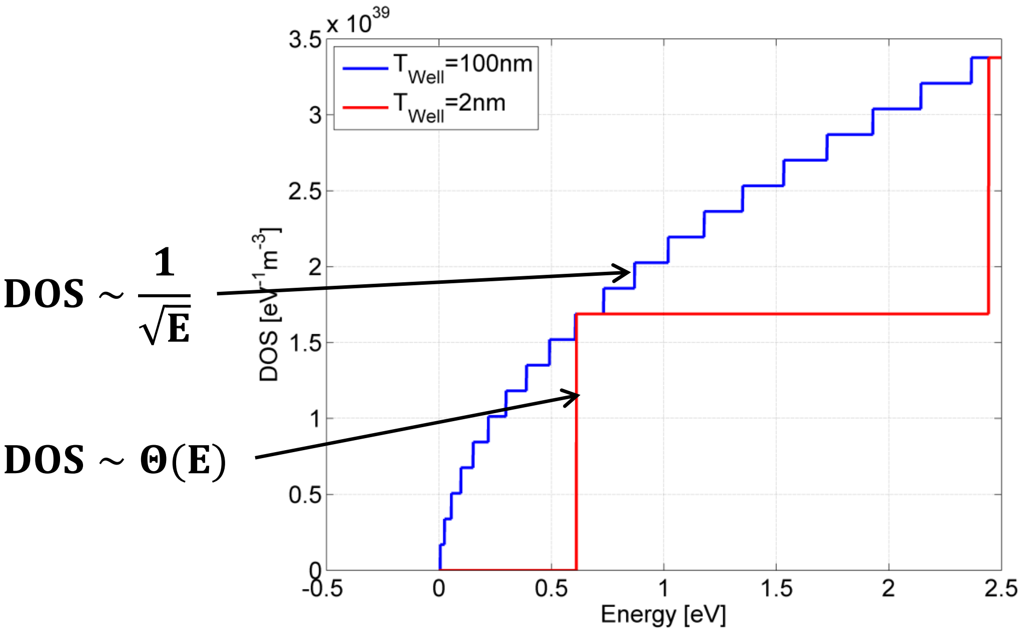
Energy band diagram of the Tunnel FET tunneling junction

Three factors affect the SS steepness:

- Barrier transparency shape **(I)**
  → $T_t(E)$
- Fermi "window" shape/position **(II)**
  → $f_v^s(E) - f_c^{ch}(E)$
- Density of states overlap **(III)**
  → $D_V^s(E) D_C^{ch}(E)$

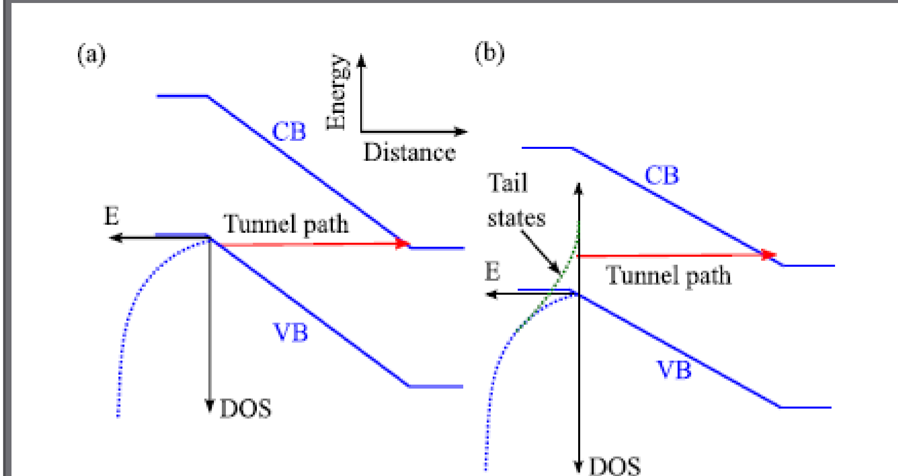
Effect of dimensionality on DOS distribution

Q: Is a 1mV/dec slope achievable by using the discretization of energy levels in highly quantized 1D or 2D structures?



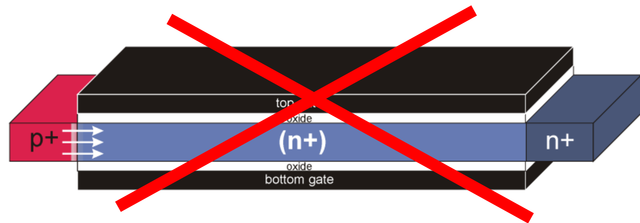
Band-tail effect is neglected

What is band-tail effect?

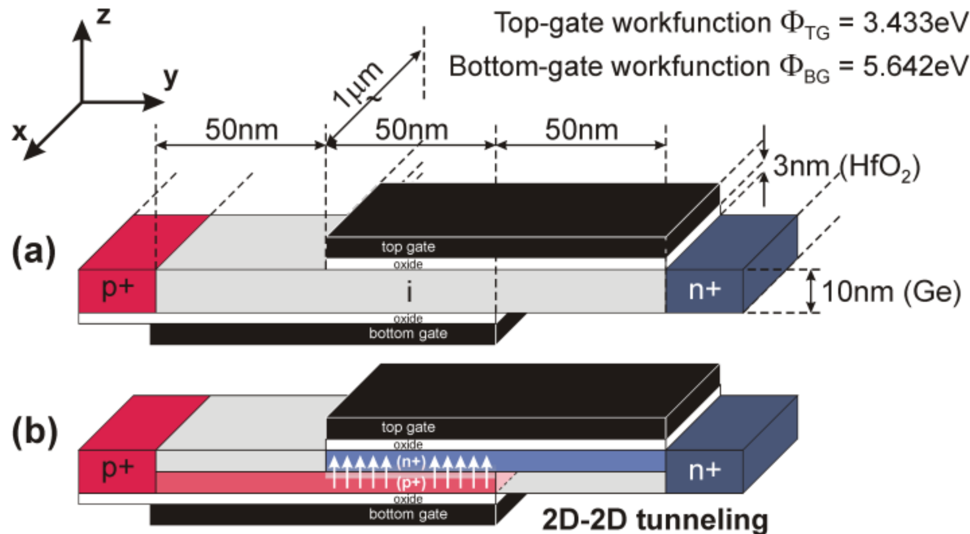


Schematic band edge diagram of a semiconductor at the onset of BTBT:
(a) in the absence of band tails;
(b) when valence band tails are present.
In the latter case, the onset of BTBT is less sharp because of the gradual increase of DOS.

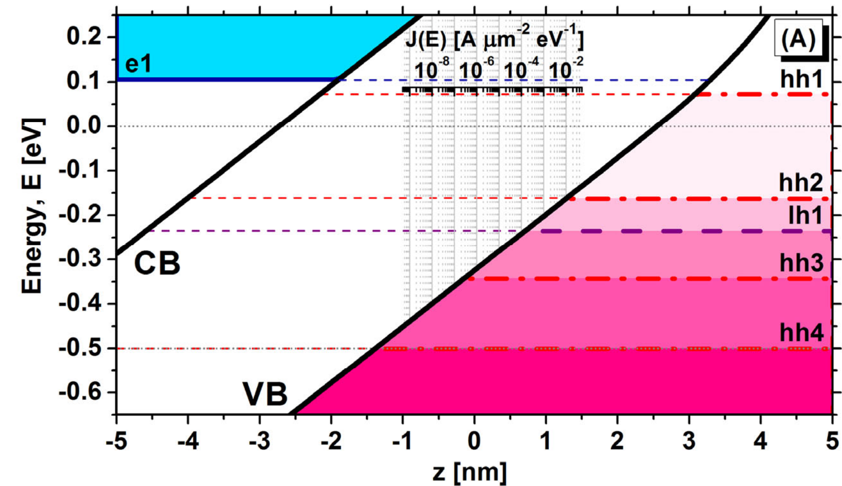
Electron-Hole Bilayer Tunnel FET (1)

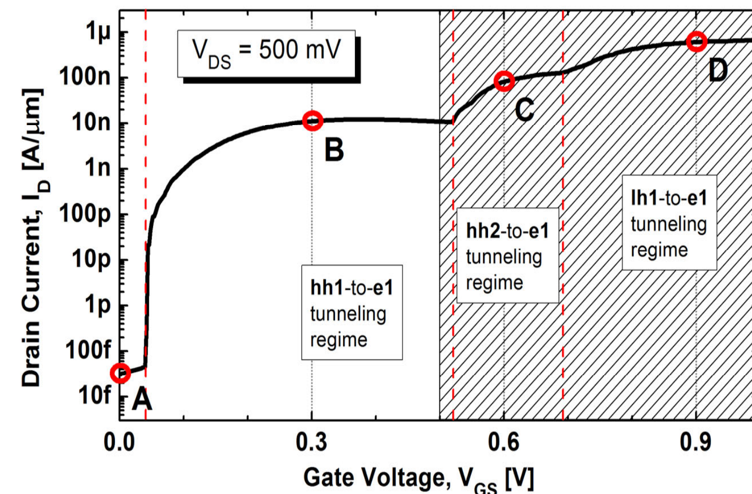


- Vertical tunneling through **a bias-induced electron-hole bilayer!**
- Complementary design (n and p) based on same device



Lattanzio & Ionescu, IEEE EDL 2012

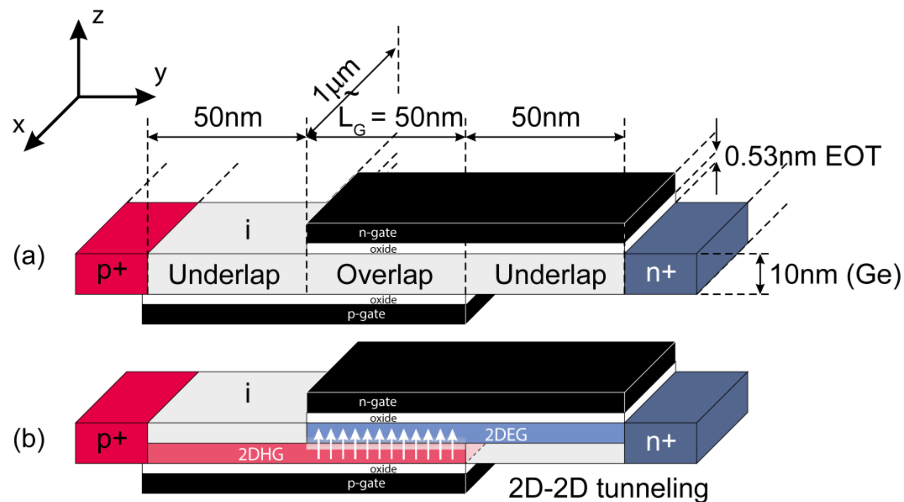


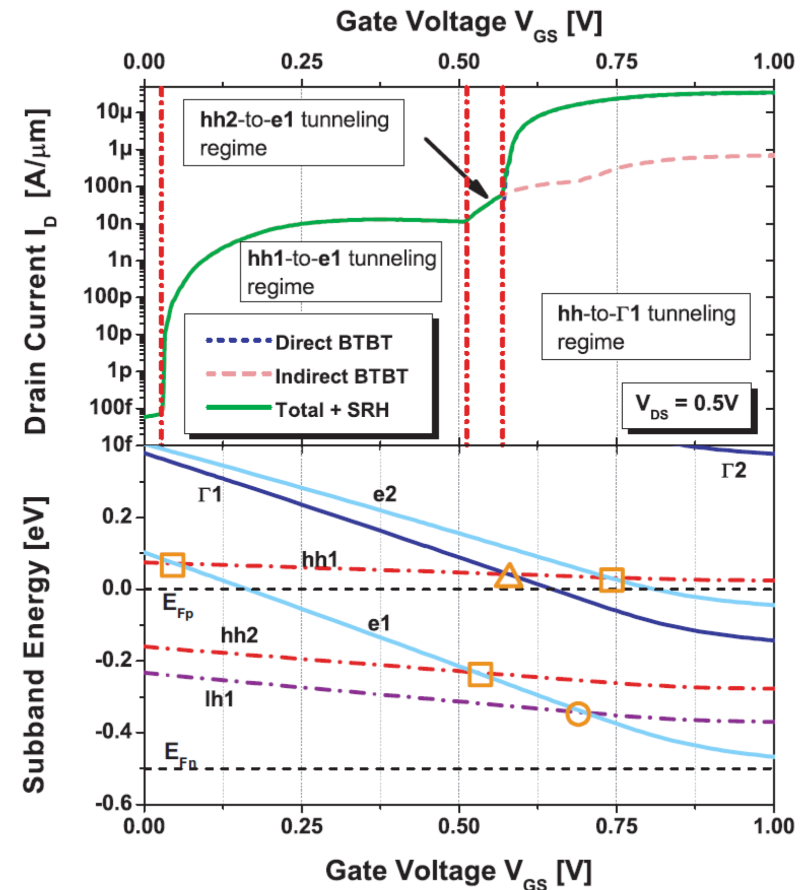


Model by Vandenberghe et al., IEDM 2011

Electron-Hole Bilayer Tunnel FET (2)

- subband-to-subband tunneling simulation (direct and indirect components) as conduction mechanism
- SRH leakage component should be avoided





A very steep increase in current is expected once the quantized energy levels of the electrons and hole align! (1-D simulations)

Alper et al., TED 2013

Electron-Hole Bilayer Tunnel FET: better than MOSFET below 0.25V

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 11, NOVEMBER 2012

On the Static and Dynamic Behavior of the Germanium Electron-Hole Bilayer Tunnel FET

Livio Lattanzio, Nilay Dağtekin, *Student Member, IEEE*, Luca De Michielis, *Student Member, IEEE*, and Adrian M. Ionescu, *Senior Member, IEEE*

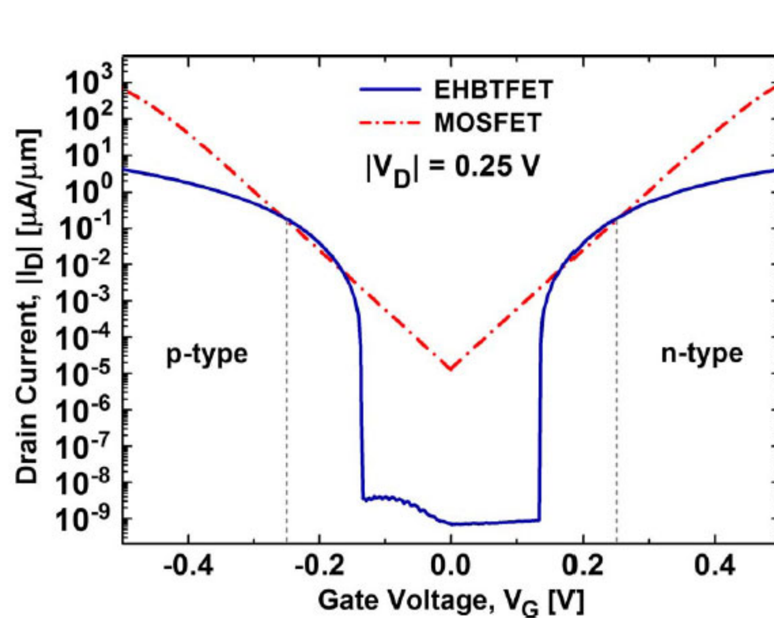


Fig. 2. Transfer characteristics (I_D–V_G) of complementary n-type ($V_G >$ 0 V) and p-type ($V_G < 0$ V) Ge EHBTFETs and MOSFETs at $|V_D| = 0.25$ V. At same $|I_{ON}| \sim 0.18$ μA/μm, the EHBTFET shows an average SS of 30 mV/dec versus 60 mV/dec of MOSFET. The EHBTFET I_{ON} can be increased further by a simple I_D–V_G shift, keeping the same leakage level. The same does not apply for the MOSFET.

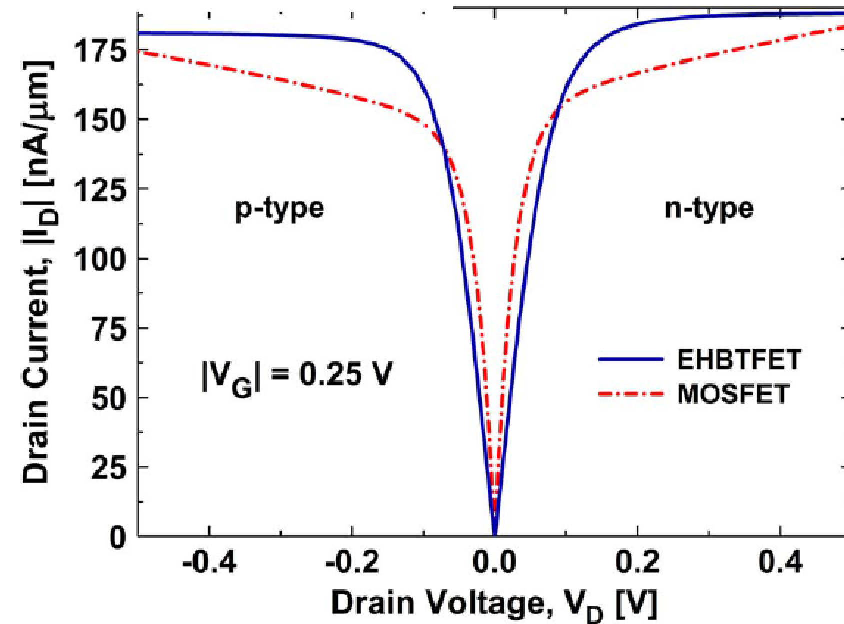
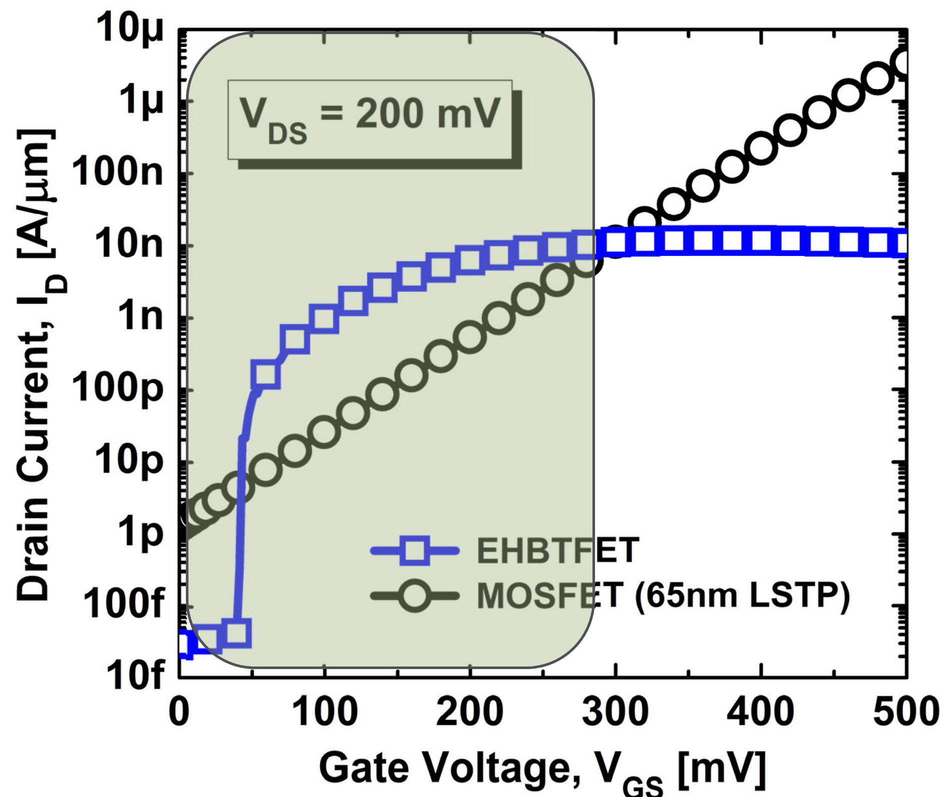
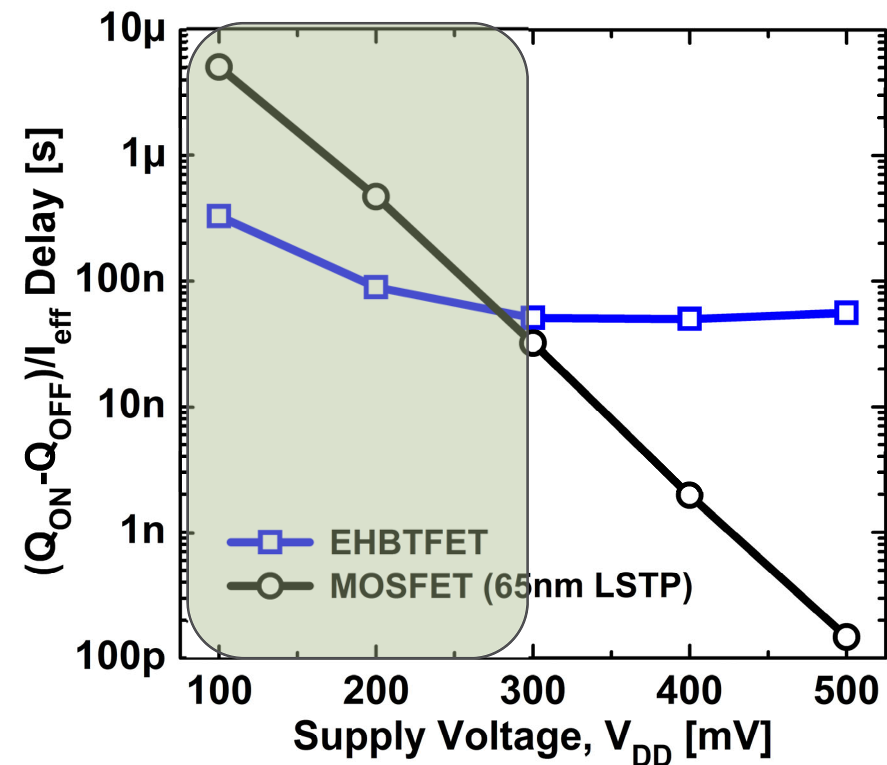


Fig. 3. Output characteristics (I_D–V_D) of complementary n-type ($V_D >$ 0 V) and p-type ($V_D < 0$ V) Ge EHBTFETs and MOSFETs at $|V_G| =$ 0.25 V. While the MOSFET is affected by SCEs and presents channel length modulation, the EHBTFET is immune and shows good saturation at high $|V_D|$. In addition, it is not presenting any superlinear behavior at low $|V_D|$.

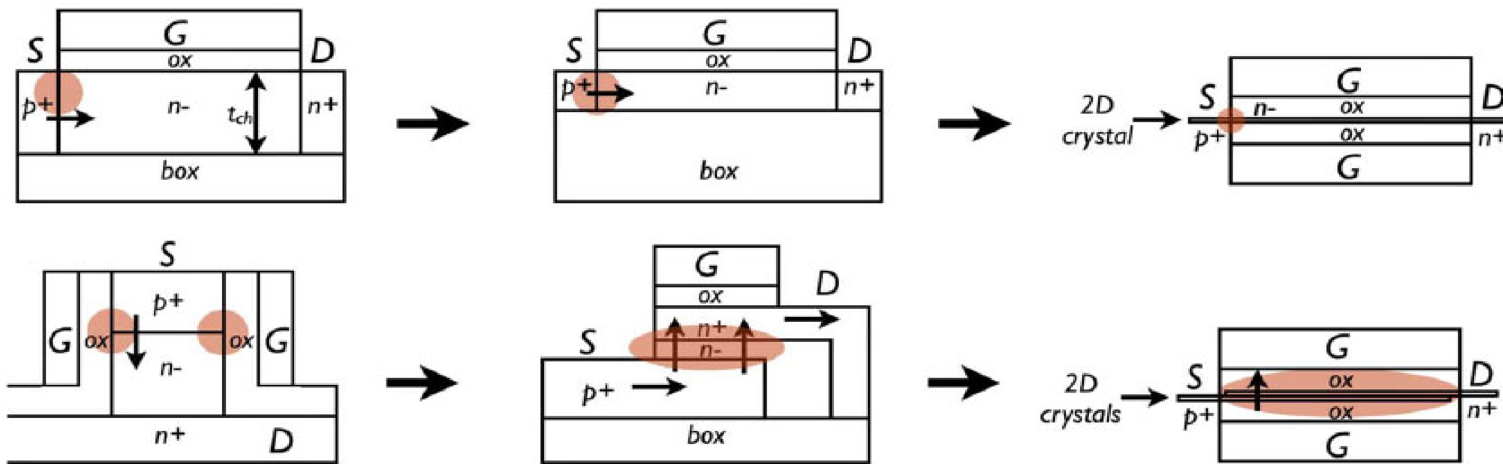
Electron-Hole Bilayer Tunnel FET below 0.25V

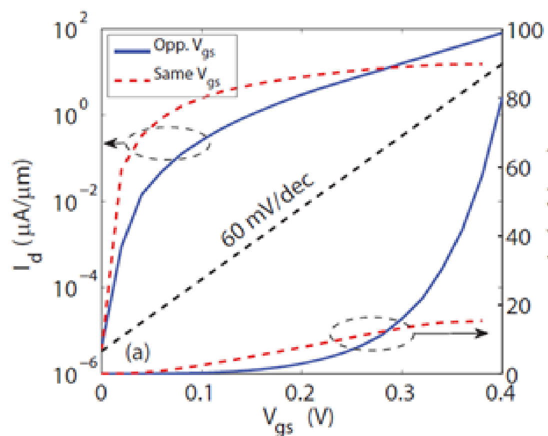
Ultra-low V_{DD} applications: EHBTFET potentially better than MOSFET for V_{DD} < 0.3V (*better Ion, smaller delay time*)



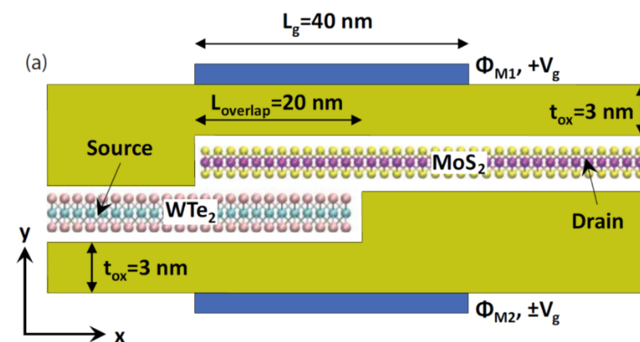


From lateral to vertical 2D Tunnel FETs using 2D semiconductors





- MoS2/WTe2 vertical junction, with strain
- Ion = 80uA/um @ Vdd=0.4V.



Szabo, Koester, Luisier, DRC 2014.

Analog Tunnel FET

Outstanding analog features compared to CMOS:

- **higher gain** @ ultra low current levels, $\mathbf{g_m/I_d > 40V^{-1}}$
- **higher unity gain frequency per unit power** for low current
- **reduced temperature dependence** of swing S, and of (maximum) transconductance, g_{max}

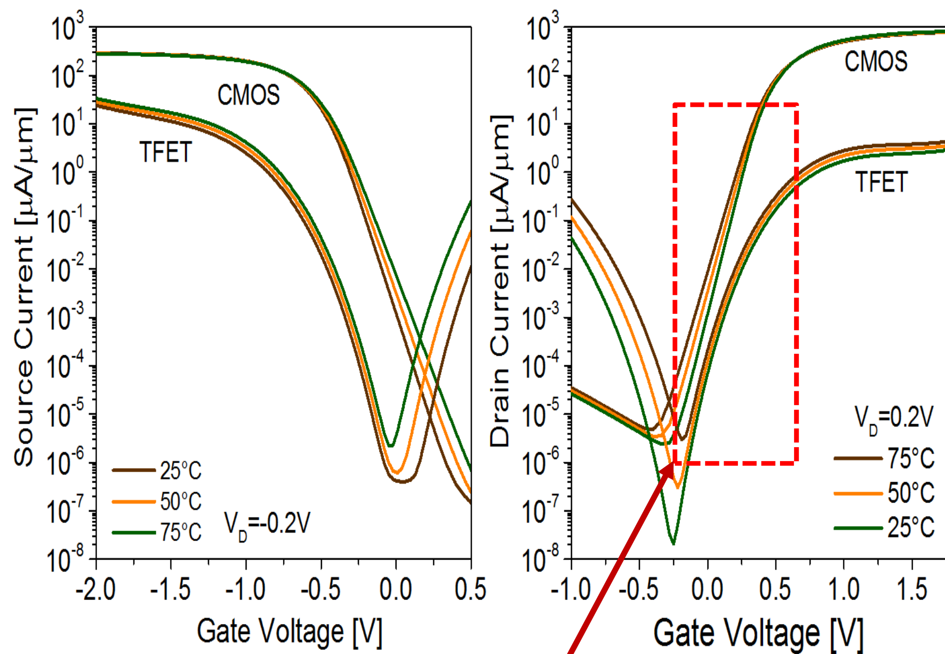
$$\frac{1}{SS} = \frac{\Delta \log_{10} I_{DS}}{\Delta V_{GS}} = \frac{1}{\log(10)} \frac{\partial \log(I_{DS})}{\partial V_{GS}} = \frac{1}{\log(10)} \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}$$

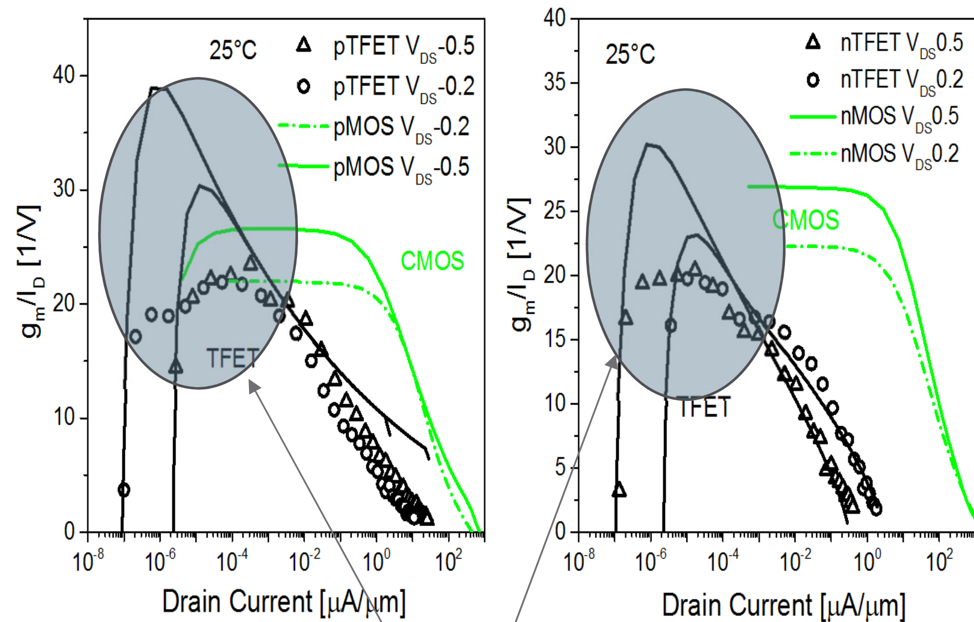
g_m

$$\frac{g_m}{I_{DS}} = \frac{\log(10)}{SS}$$

- Limit of **40V^{-1}** (for SS=60mV/dec @ RT) in CMOS.
- Transconductance efficiency measures how much transconductance is produced for a given bias current; important for ***amplifier design***.

28nm Complementary Tunnel FETs versus FDSOI CMOS: comparison



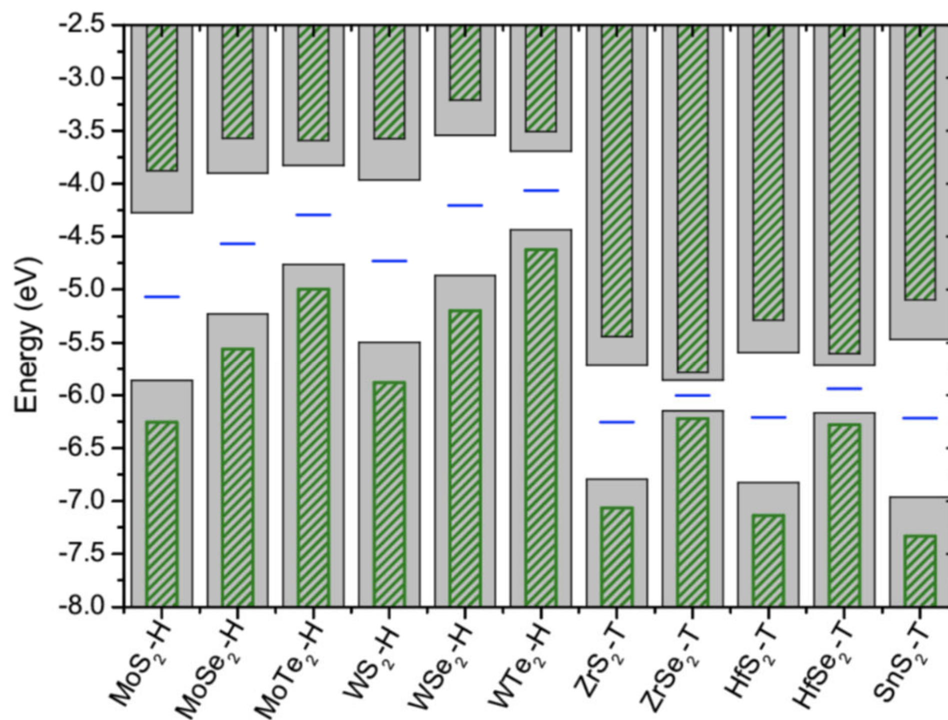


Tunnel FET is more stable in temperature as temperature dependence of BTBT is low (only via the low linear bandgap dependence on temperature).

Higher gm/Id at low current: excellent for low power analog amplifier design.

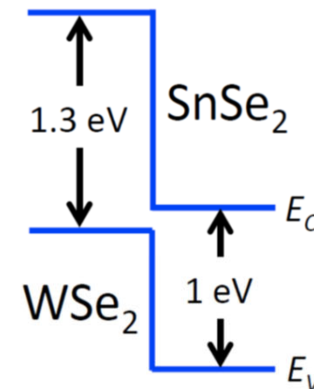
Other solutions?
Any material heaven for Tunnel FETs?

Band gap heaven - 2D crystal band alignments



Calculated by density functional theory

preferred band alignments for TFETs



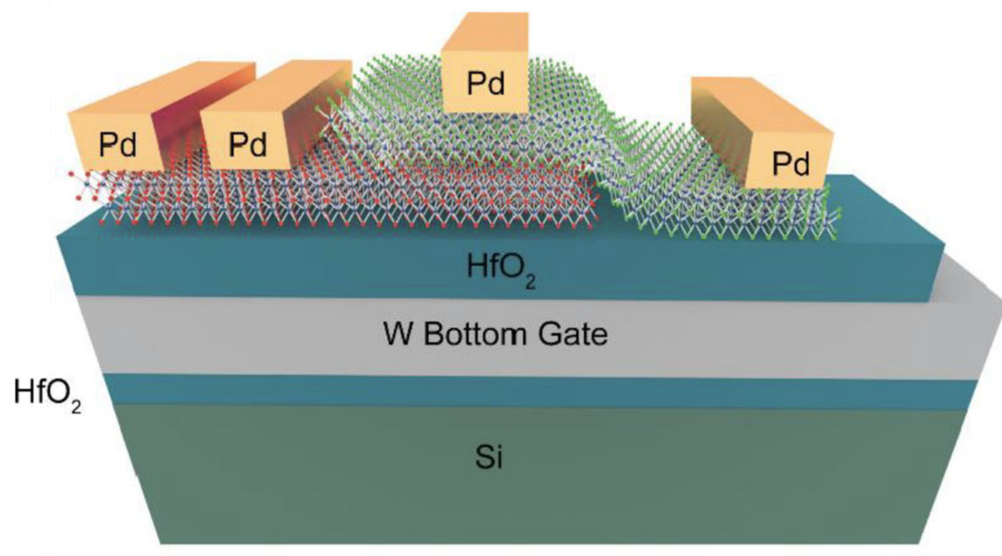
Two transport options

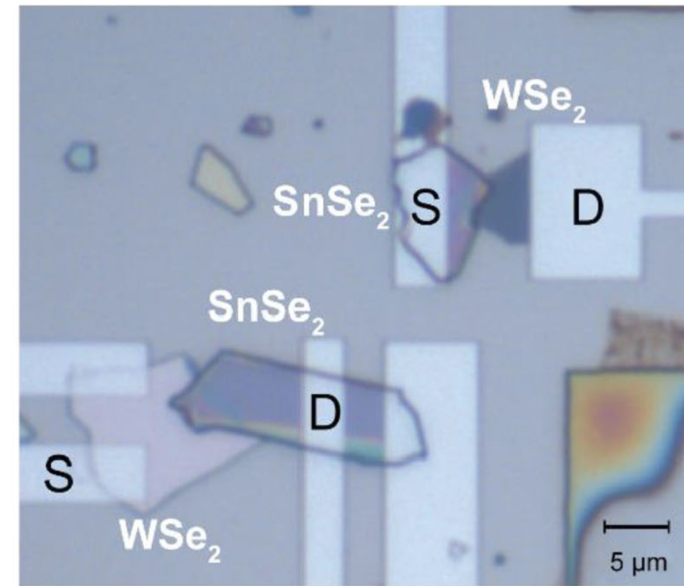
in-plane

interlayer

Device structure: bottom gated $WSe_2/SnSe_2$

- Deterministic assembly of $WSe_2/SnSe_2$ heterojunction
- Depending on flake size, one to two contacts per material





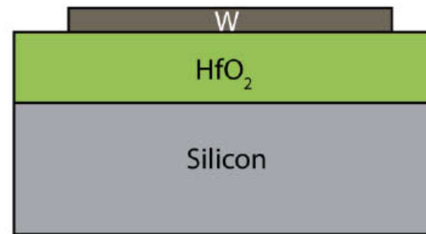
Nicolo Oliva et al, @ Iedm 2019.

Process flow

a)

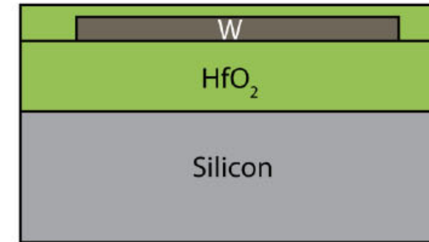
HfO_2 ALD

b)



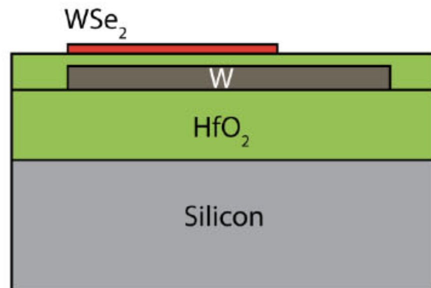
W BG lift-off

c)



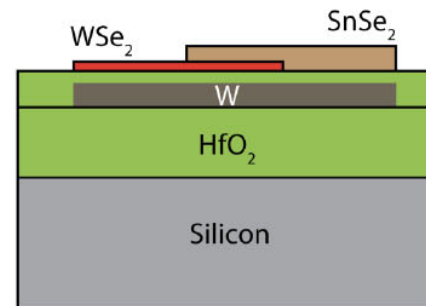
HfO_2 ALD

d)



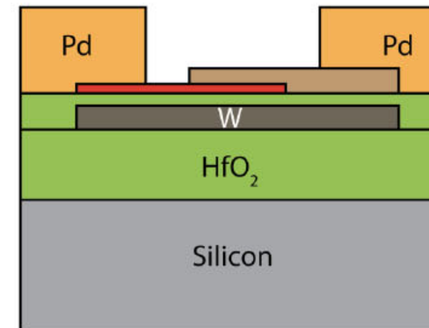
WSe_2 exfoliation and $SnSe_2$ transfer

e)



$SnSe_2$ deterministic transfer

f)

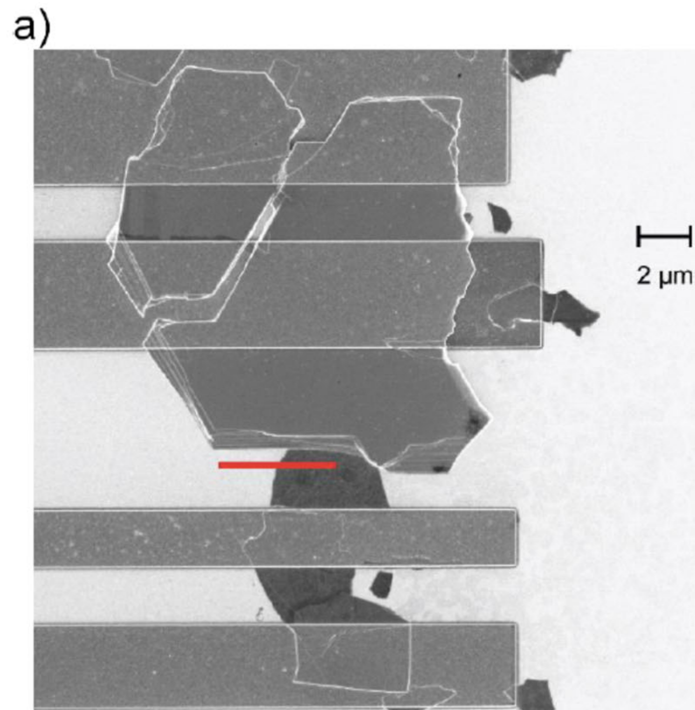


Pd contacts lift-off

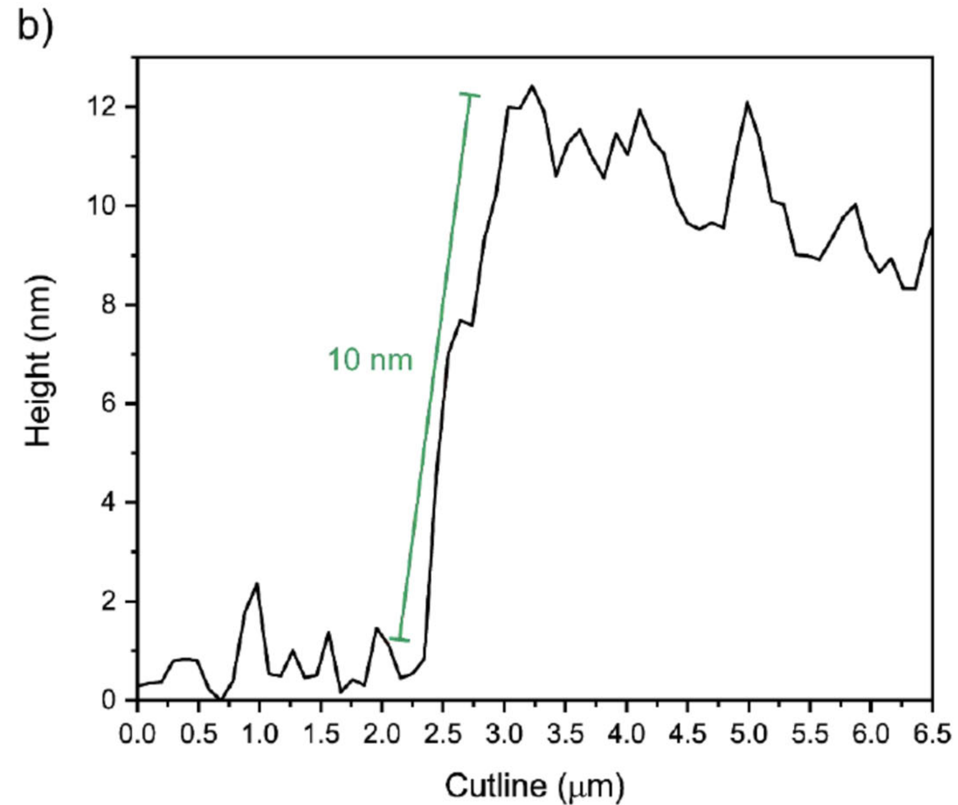
Device structure: metrology

- Clean, sharp interface on high quality bottom gate dielectric

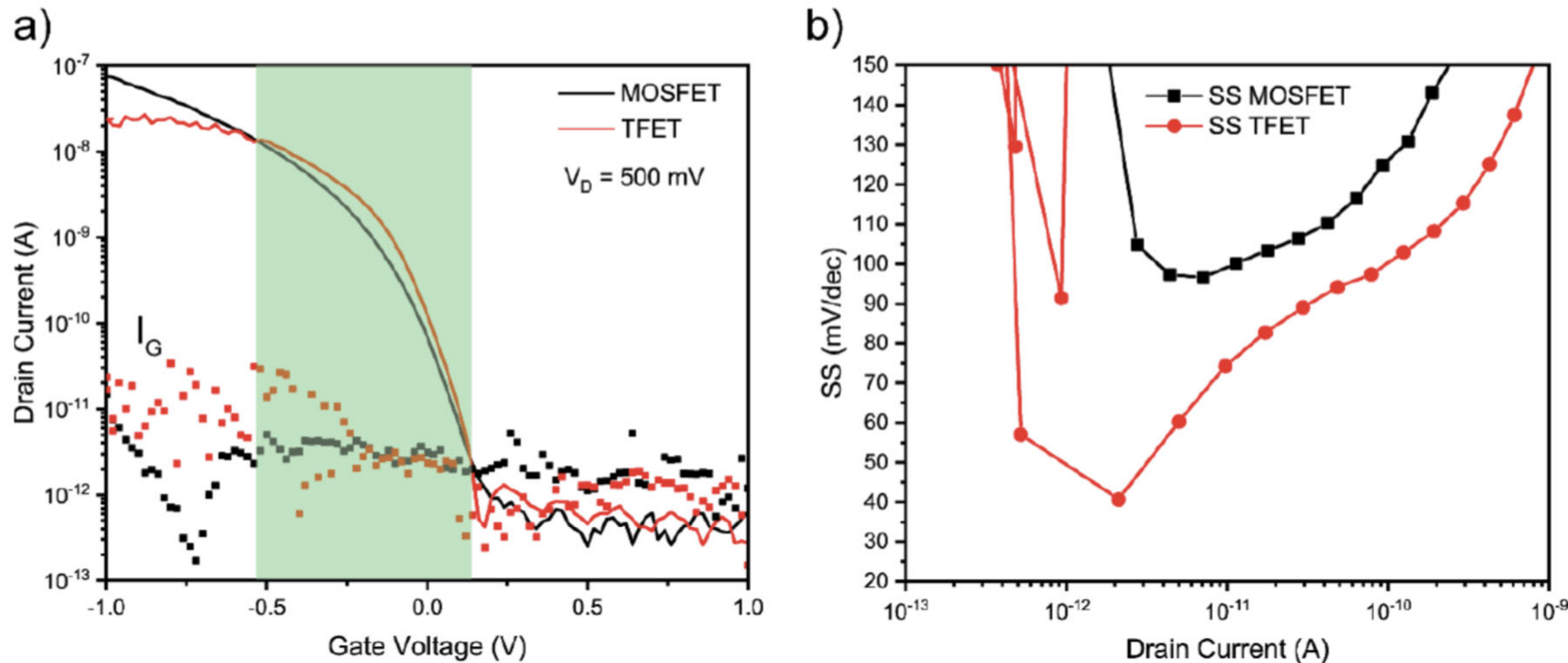
a)



b)



TFET 2 vs MOSFET 2 on *same* flake



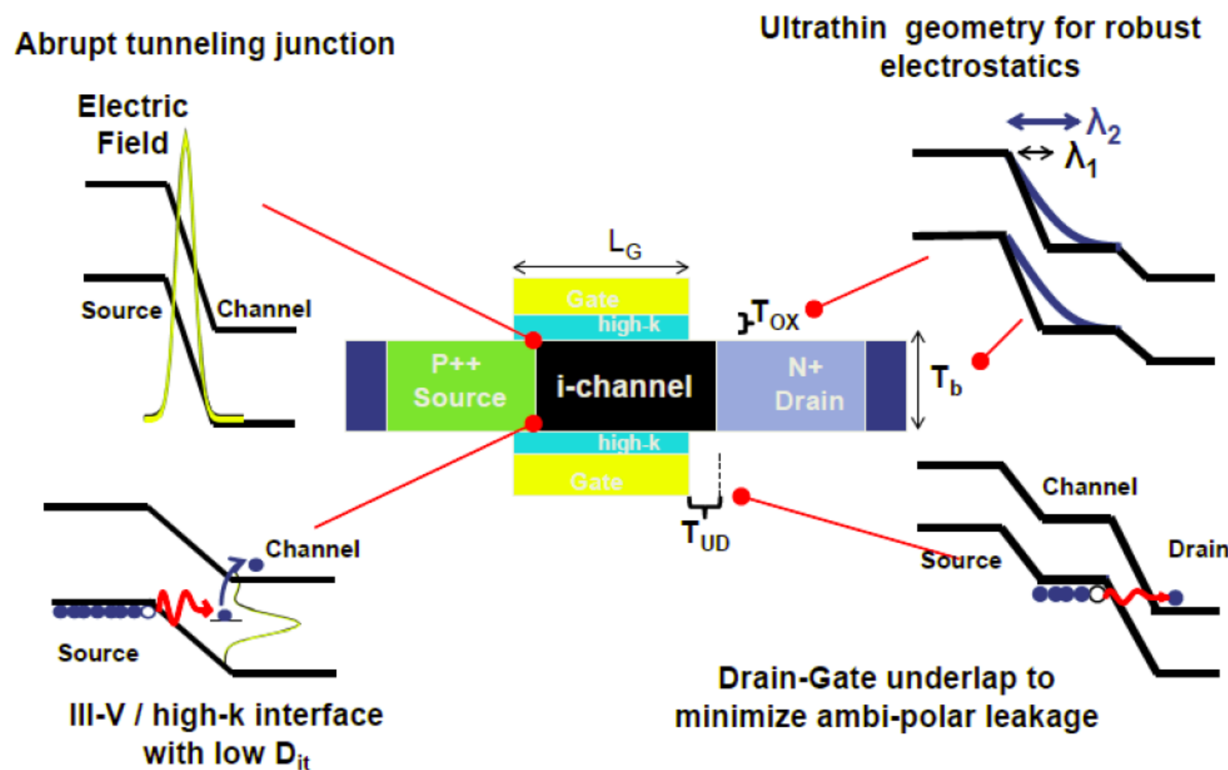
- TFET 2 outperforms its built-in MOSFET over three orders of I_D

WSe 2/SnSe 2 vdW heterojunction Tunnel FET with subthermionic characteristic and MOSFET co-integrated on same WSe 2 flake
N Oliva, J Backman, L Capua, M Cavalieri, M Luisier, AM Ionescu, npj 2D Materials and Applications, 2020.

Conclusions (1): steep slope tunnel FETs

- **Many remaining challenges of making a good tunnel FET**

more difficult than for making a good MOSFET but the new operation and design space below 0.3V is crucial for future energy efficient electronics



Conclusions (2): steep slope tunnel FETs

Tunnel FET: most promising steep slope switch to reduce the supply voltage below 0.5 V and offer significant power savings

Technological challenges:

- Optimized Complementary technology : heterostructure Tunnel FET exploiting III-V on silicon and strained (Si)Ge source devices
- Optimization of dynamic/transient regime
- Parameter sensitivity and variability

New concepts like the Density-of-States (DOS) switch offer paths for a sub-10mV/dec slope at RT and sub-0.1V operation

New conceptual and design challenges:

- **Simulation and modeling tools**
- **Selection of most appropriate material system embodiment**
- **Optimization of design for avoid leakage**

New Heaven for Tunnel FETs: 2D-2D vdW structures!